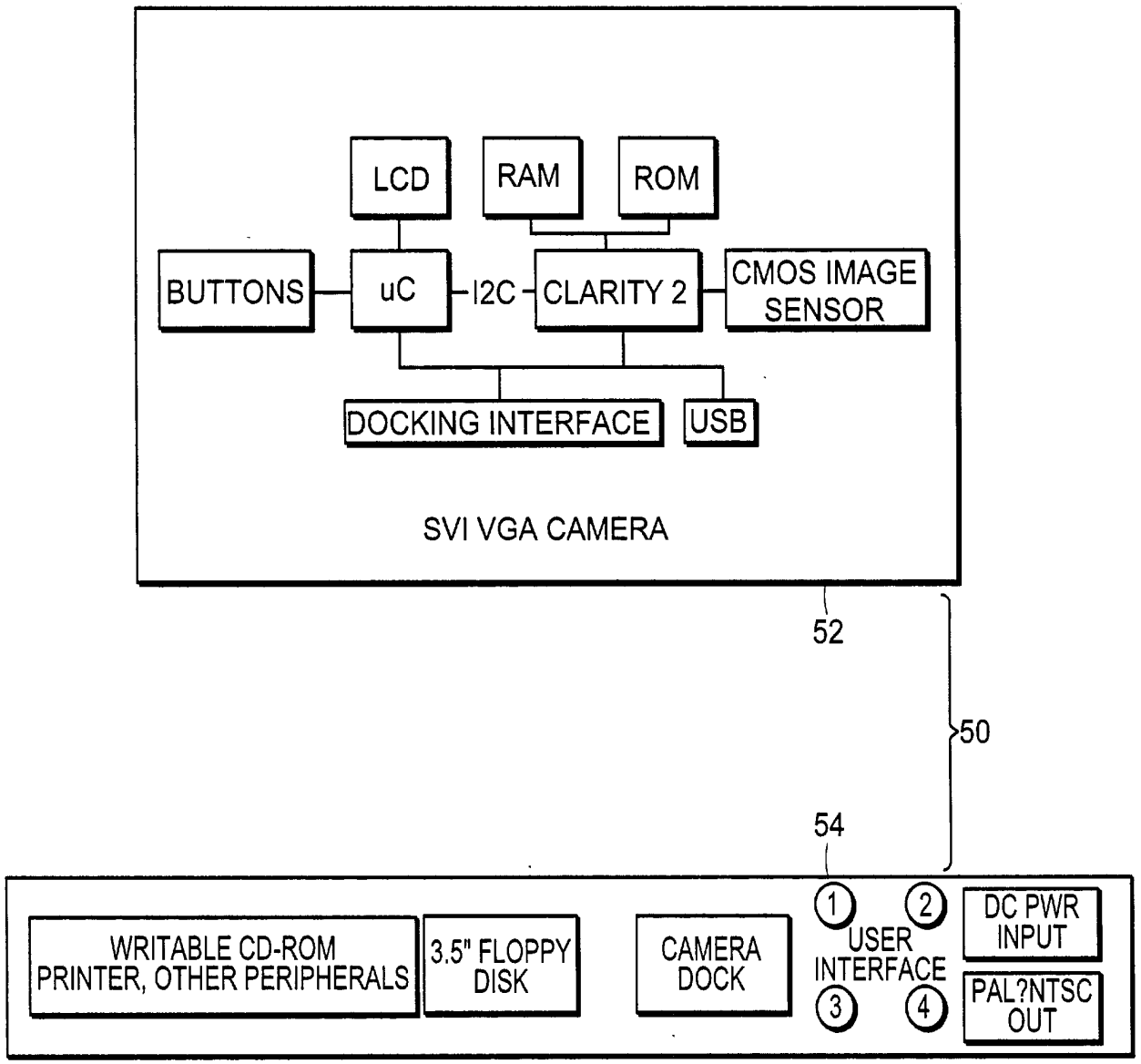

LCD
RAM
ROM
BUTTONS
uC
I2C
CLARITY 2
CMOS IMAGE SENSOR
DOCKING INTERFACE
USB
SVI VGA CAMERA
52
50
54
WRITABLE CD-ROM PRINTER, OTHER PERIPHERALS
3.5" FLOPPY DISK
CAMERA DOCK
1
2
USER INTERFACE
3
4
DC PWR INPUT
PAL?NTSC OUT
SVI DOCKING STATION

FIG. 1

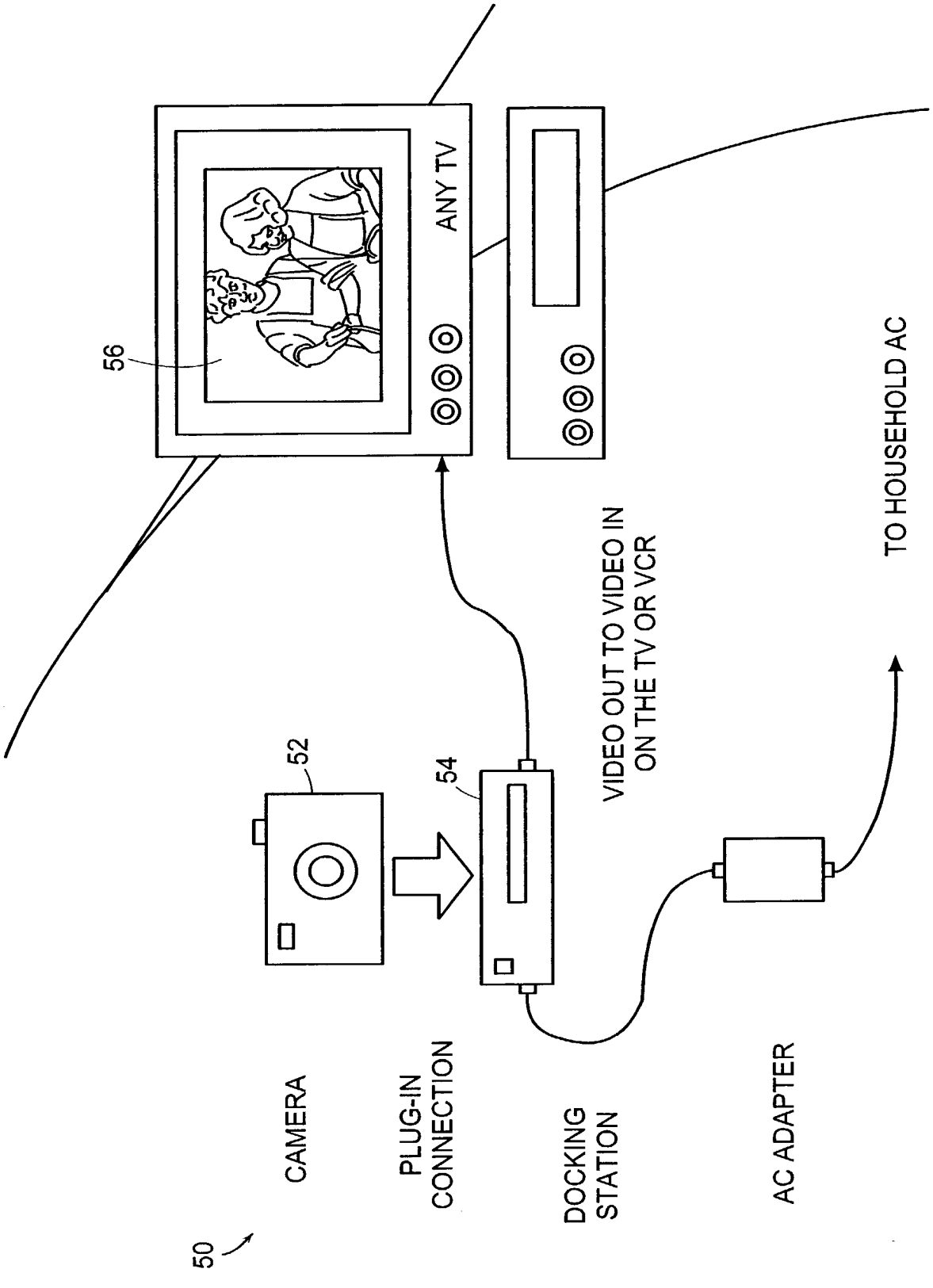

ANY TV
56
TO HOUSEHOLD AC
VIDEO OUT TO VIDEO IN
ON THE TV OR VCR
52
54
50
CAMERA
PLUG-IN
CONNECTION
DOCKING
STATION
AC ADAPTER

FIG. 2

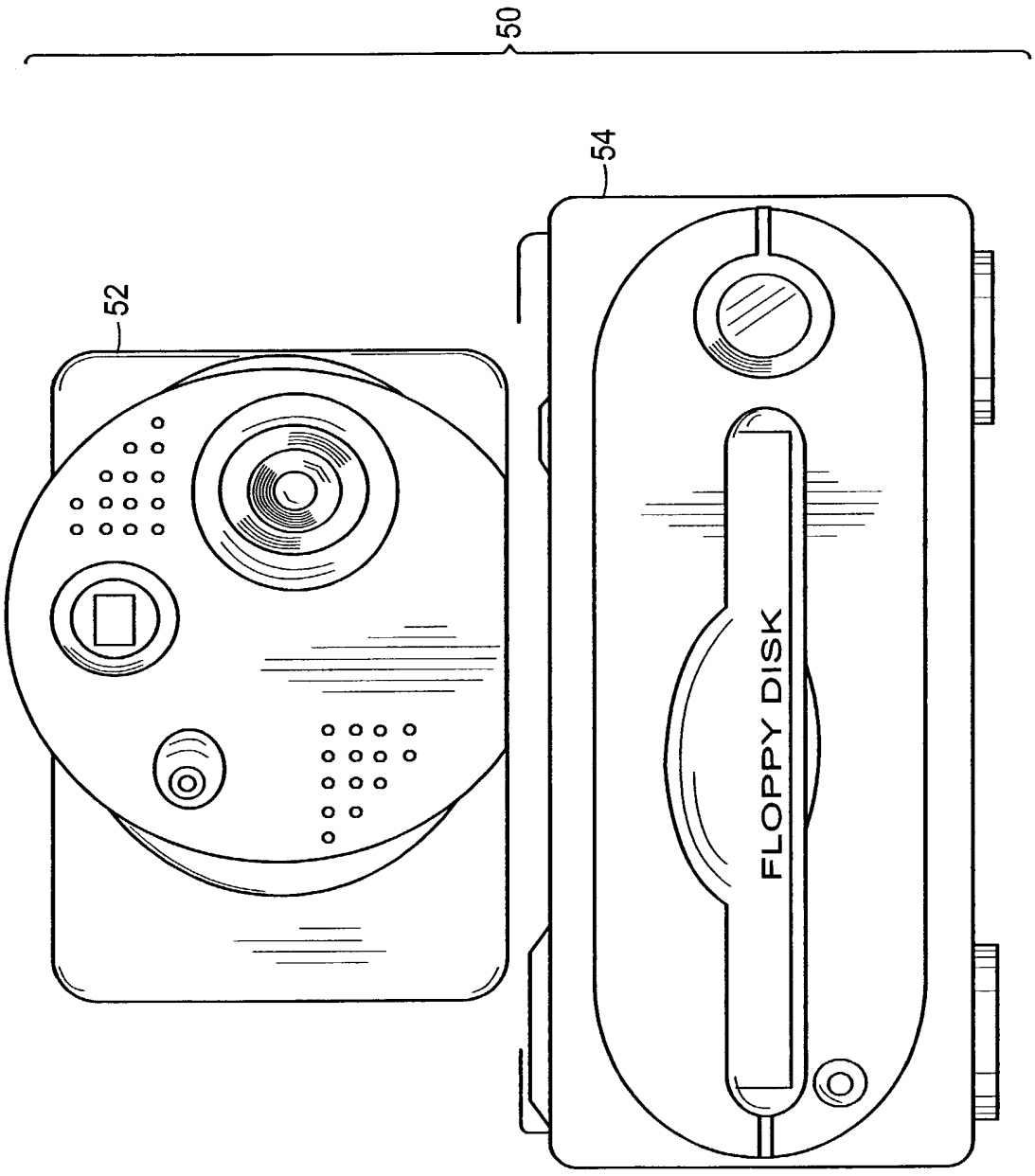


FIG. 3

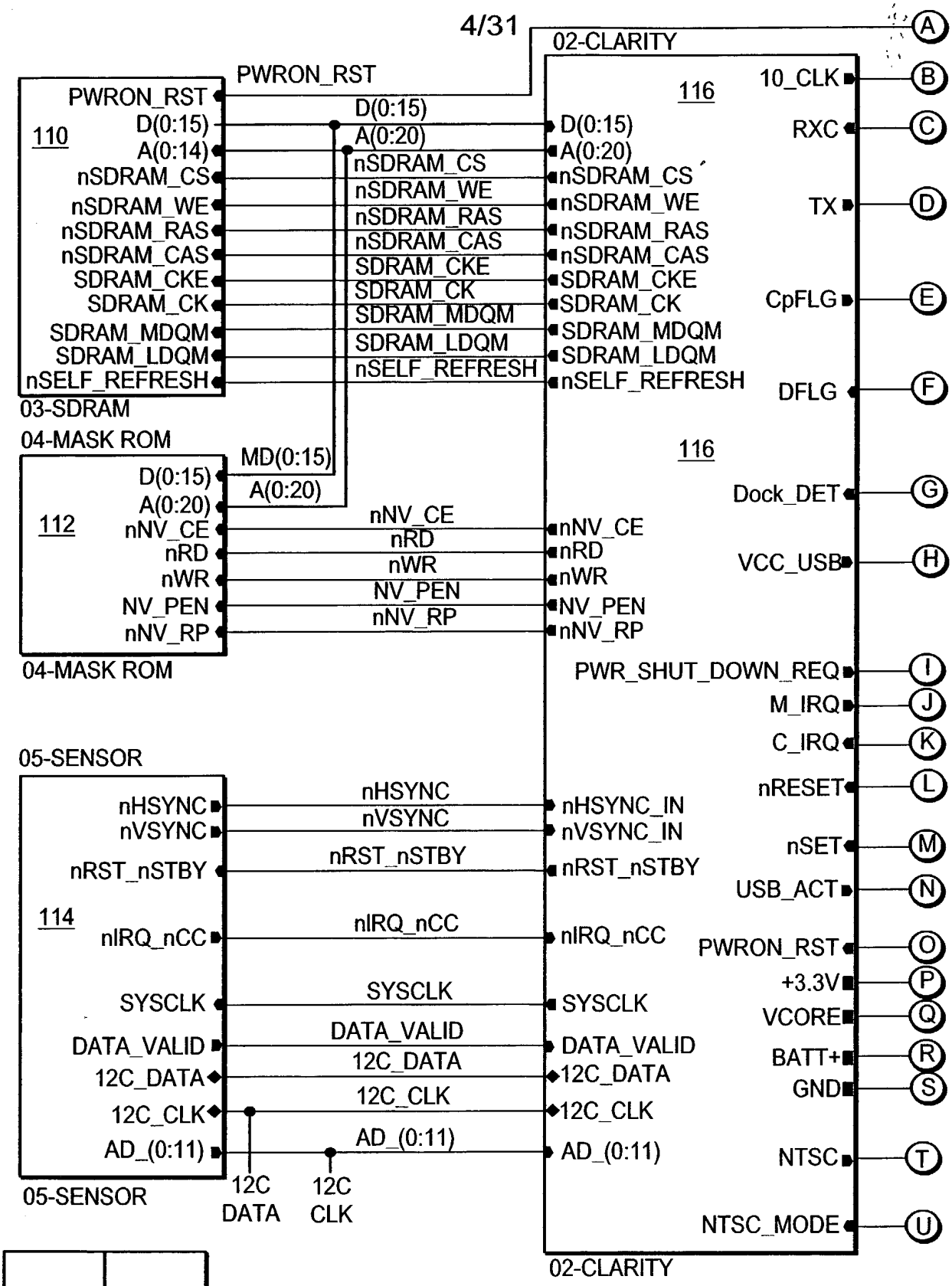


FIG. 4A

FIG. 4A | FIG. 4B

FIG. 4

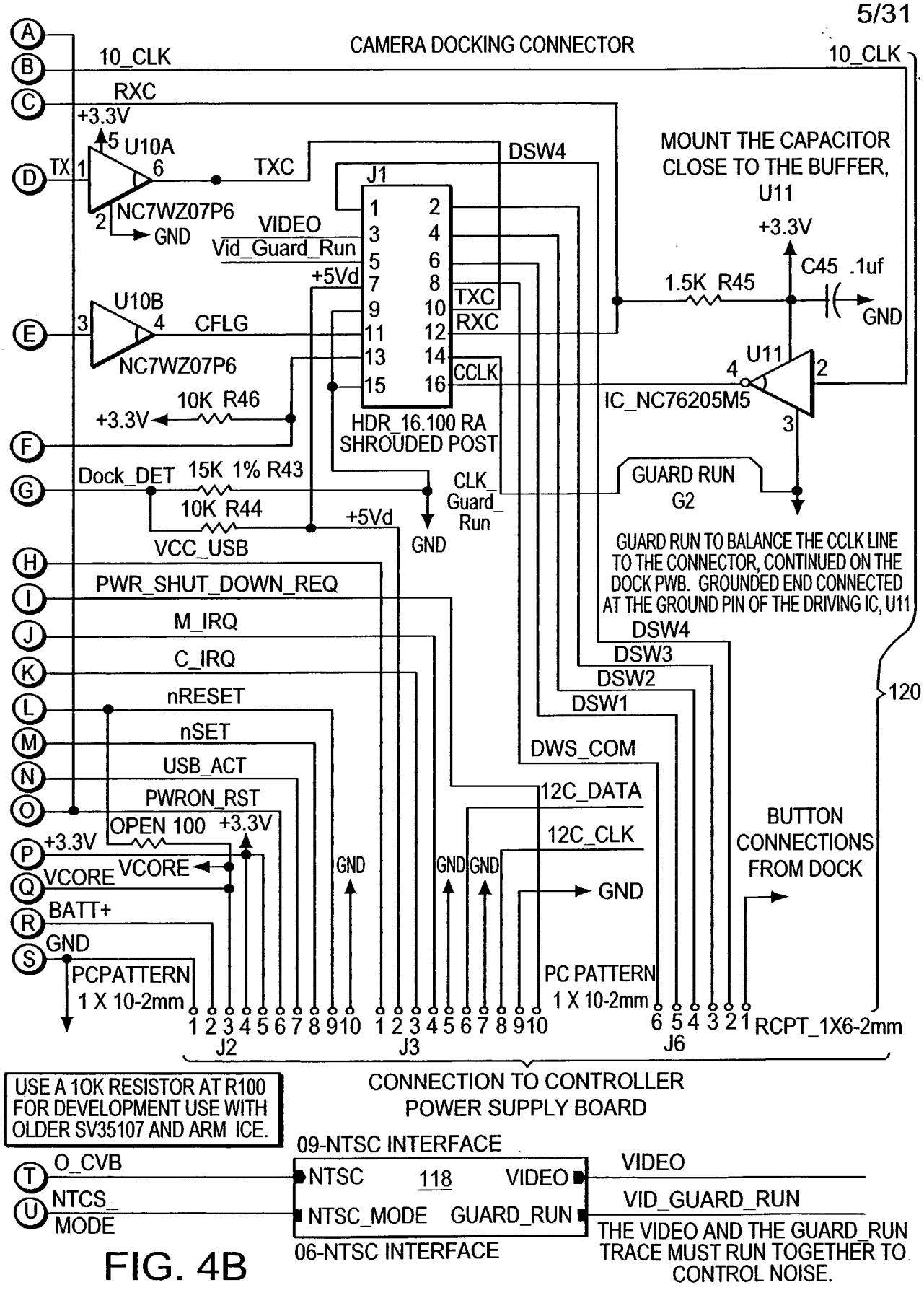

CAMERA DOCKING CONNECTOR
10_CLK
RXC
+3.3V
U10A
NC7WZ07P6
TX
TXC
GND
VIDEO
Vid_Guard_Run
+5Vd
U10B
CFLG
10K R46
J1
HDR_16.100 RA
SHROUDED POST
DSW4
MOUNT THE CAPACITOR
CLOSE TO THE BUFFER,
U11
1.5K R45
C45 .1uf
U11
IC_NC76205M5
GUARD RUN
G2
Dock_DET
15K 1% R43
10K R44
VCC_USB
CLK_
Guard_
Run
GUARD RUN TO BALANCE THE CCLK LINE
TO THE CONNECTOR, CONTINUED ON THE
DOCK PWB. GROUNDED END CONNECTED
AT THE GROUND PIN OF THE DRIVING IC, U11
PWR_SHUT_DOWN_REQ
M_IRQ
C_IRQ
nRESET
nSET
USB_ACT
PWRON_RST
OPEN 100
DSW3
DSW2
DSW1
DWS_COM
12C_DATA
12C_CLK
120
BUTTON
CONNECTIONS
FROM DOCK
VCORE
BATT+
PCPATTERN
1 X 10-2mm
PC PATTERN
1 X 10-2mm
RCPT_1X6-2mm
J2
J3
J6
USE A 10K RESISTOR AT R100
FOR DEVELOPMENT USE WITH
OLDER SV35107 AND ARM ICE.
CONNECTION TO CONTROLLER
POWER SUPPLY BOARD
09-NTSC INTERFACE
O_CVB
NTCS_
MODE
NTSC
118
VIDEO
NTSC_MODE
GUARD_RUN
06-NTSC INTERFACE
VIDEO
VID_GUARD_RUN
THE VIDEO AND THE GUARD_RUN
TRACE MUST RUN TOGETHER TO
CONTROL NOISE.

FIG. 4B

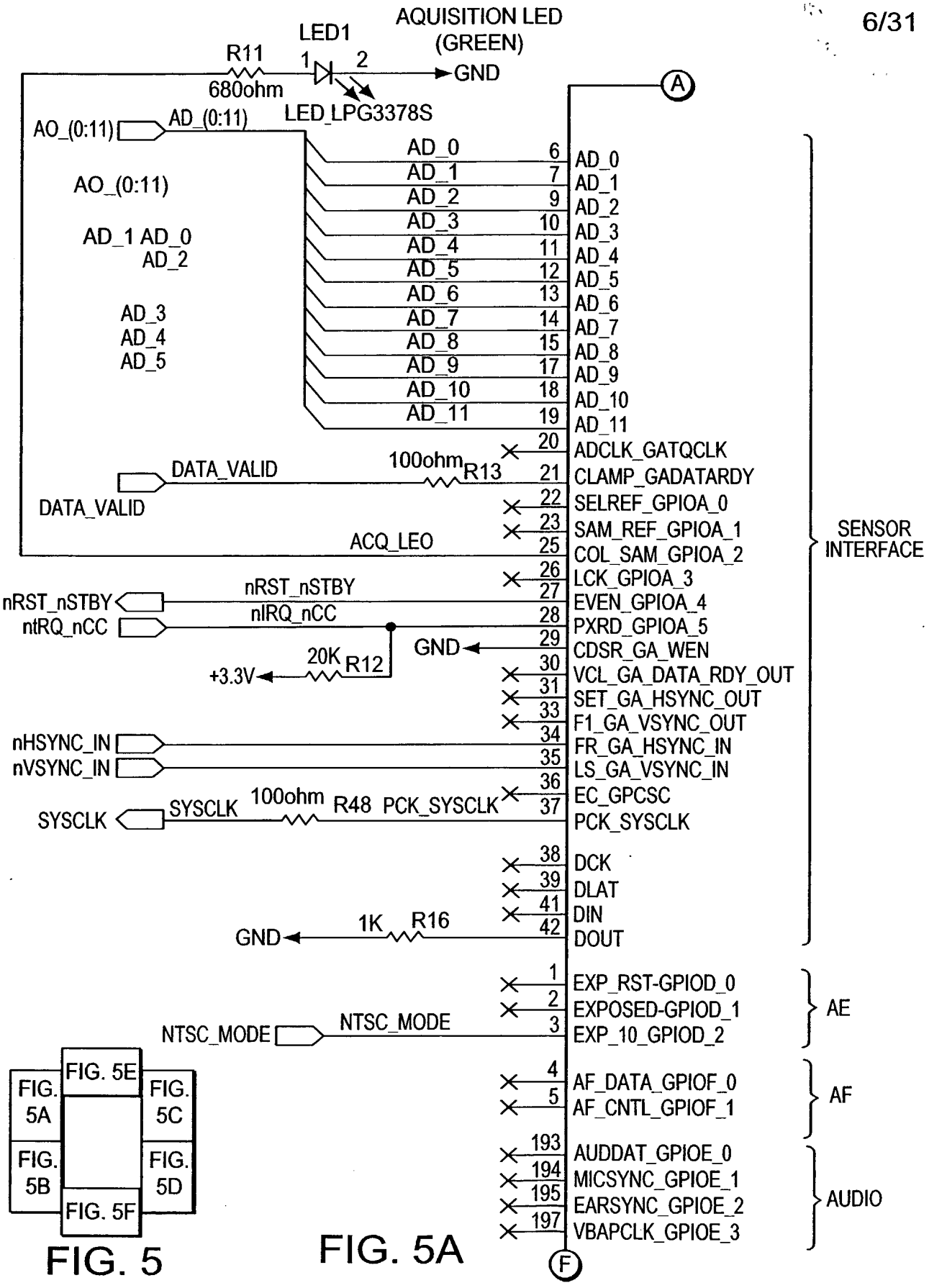

AQUISITION LED
(GREEN)
LED1
R11
680ohm
LED_LPG3378S
GND
AO_(0:11)
AD_(0:11)
AD_0
AD_1
AD_2
AD_3
AD_4
AD_5
AD_6
AD_7
AD_8
AD_9
AD_10
AD_11
ADCLK_GATQCLK
DATA_VALID
100ohm
R13
CLAMP_GADATARDY
SELREF_GPIOA_0
SAM_REF_GPIOA_1
ACQ_LEO
COL_SAM_GPIOA_2
LCK_GPIOA_3
nRST_nSTBY
EVEN_GPIOA_4
nIRQ_nCC
PXRD_GPIOA_5
20K
R12
+3.3V
CDSR_GA_WEN
VCL_GA_DATA_RDY_OUT
SET_GA_HSYNC_OUT
F1_GA_VSYNC_OUT
nHSYNC_IN
nVSYNC_IN
FR_GA_HSYNC_IN
LS_GA_VSYNC_IN
EC_GPCSC
SYSCLK
100ohm
R48
PCK_SYSCLK
DCK
DLAT
DIN
1K
R16
DOUT
EXP_RST-GPIOD_0
EXPOSED-GPIOD_1
NTSC_MODE
EXP_10_GPIOD_2
AF_DATA_GPIOF_0
AF_CNTL_GPIOF_1
AUDDAT_GPIOE_0
MICSYNC_GPIOE_1
EARSYNC_GPIOE_2
VBAPCLK_GPIOE_3
SENSOR INTERFACE
AE
AF
AUDIO
A
F

FIG. 5A

FIG. 5E
FIG. 5A
FIG. 5C
FIG. 5B
FIG. 5D
FIG. 5F

FIG. 5

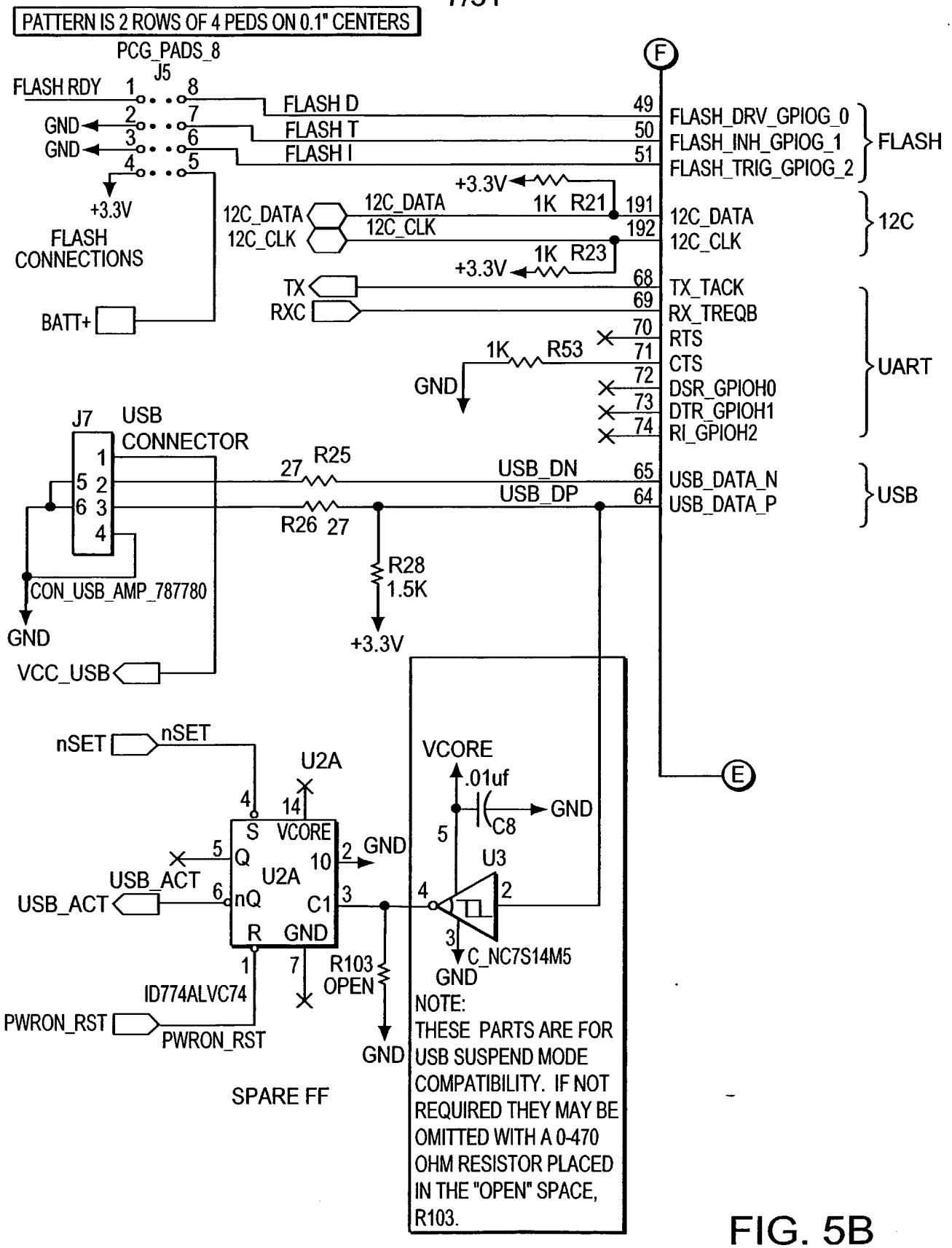

PATTERN IS 2 ROWS OF 4 PEDS ON 0.1" CENTERS
PCG_PADS_8
J5
FLASH RDY
GND
GND
+3.3V
FLASH CONNECTIONS
BATT+
FLASH D
FLASH T
FLASH I
12C_DATA
12C_CLK
+3.3V
1K R21
1K R23
TX
RXC
1K R53
GND
J7 USB CONNECTOR
CON_USB_AMP_787780
GND
VCC_USB
27 R25
R26 27
R28 1.5K
+3.3V
USB_DN
USB_DP
F
E
FLASH_DRV_GPIOG_0
FLASH_INH_GPIOG_1
FLASH_TRIG_GPIOG_2
FLASH
12C_DATA
12C_CLK
12C
TX_TACK
RX_TREQB
RTS
CTS
DSR_GPIOH0
DTR_GPIOH1
RI_GPIOH2
UART
USB_DATA_N
USB_DATA_P
USB
nSET
nSET
U2A
VCORE
.01uf
C8
GND
U3
C_NC7S14M5
GND
USB_ACT
USB_ACT
U2A
VCORE
GND
R GND
R103 OPEN
GND
ID774ALVC74
PWRON_RST
PWRON_RST
SPARE FF
NOTE:
THESE PARTS ARE FOR USB SUSPEND MODE COMPATIBILITY. IF NOT REQUIRED THEY MAY BE OMITTED WITH A 0-470 OHM RESISTOR PLACED IN THE "OPEN" SPACE, R103.

FIG. 5B

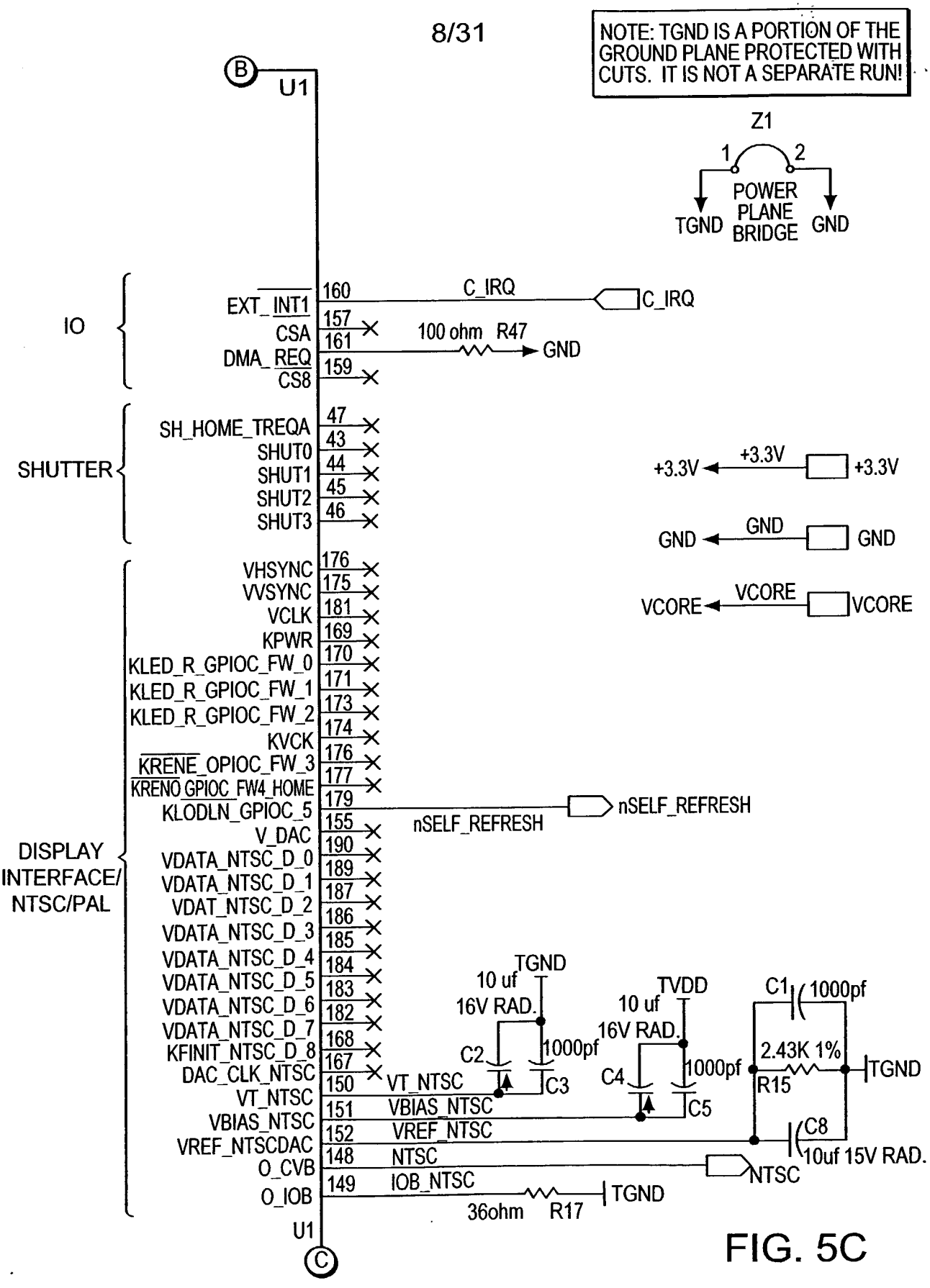

NOTE: TGND IS A PORTION OF THE GROUND PLANE PROTECTED WITH CUTS. IT IS NOT A SEPARATE RUN!
Z1
1
2
POWER PLANE BRIDGE
TGND
GND
B
U1
IO
SHUTTER
DISPLAY INTERFACE/ NTSC/PAL
EXT_INT1
CSA
DMA_REQ
CS8
SH_HOME_TREQA
SHUT0
SHUT1
SHUT2
SHUT3
VHSYNC
VVSYNC
VCLK
KPWR
KLED_R_GPIOC_FW_0
KLED_R_GPIOC_FW_1
KLED_R_GPIOC_FW_2
KVCK
KRENE_OPIOC_FW_3
KRENO GPIOC FW4 HOME
KLODLN_GPIOC_5
V_DAC
VDATA_NTSC_D_0
VDATA_NTSC_D_1
VDAT_NTSC_D_2
VDATA_NTSC_D_3
VDATA_NTSC_D_4
VDATA_NTSC_D_5
VDATA_NTSC_D_6
VDATA_NTSC_D_7
KFINIT_NTSC_D_8
DAC_CLK_NTSC
VT_NTSC
VBIAS_NTSC
VREF_NTSCDAC
O_CVB
O_IOB
160
157
161
159
47
43
44
45
46
176
175
181
169
170
171
173
174
176
177
179
155
190
189
187
186
185
184
183
182
168
167
150
151
152
148
149
C_IRQ
C_IRQ
100 ohm R47
GND
+3.3V
+3.3V
+3.3V
GND
GND
GND
VCORE
VCORE
VCORE
nSELF_REFRESH
nSELF_REFRESH
TGND
10 uf
16V RAD.
C2
1000pf
C3
VT_NTSC
VBIAS_NTSC
VREF_NTSC
NTSC
IOB_NTSC
TVDD
10 uf
16V RAD.
C4
1000pf
C5
C1
1000pf
2.43K 1%
R15
TGND
C8
10uf 15V RAD.
NTSC
36ohm R17
TGND
U1
C

FIG. 5C

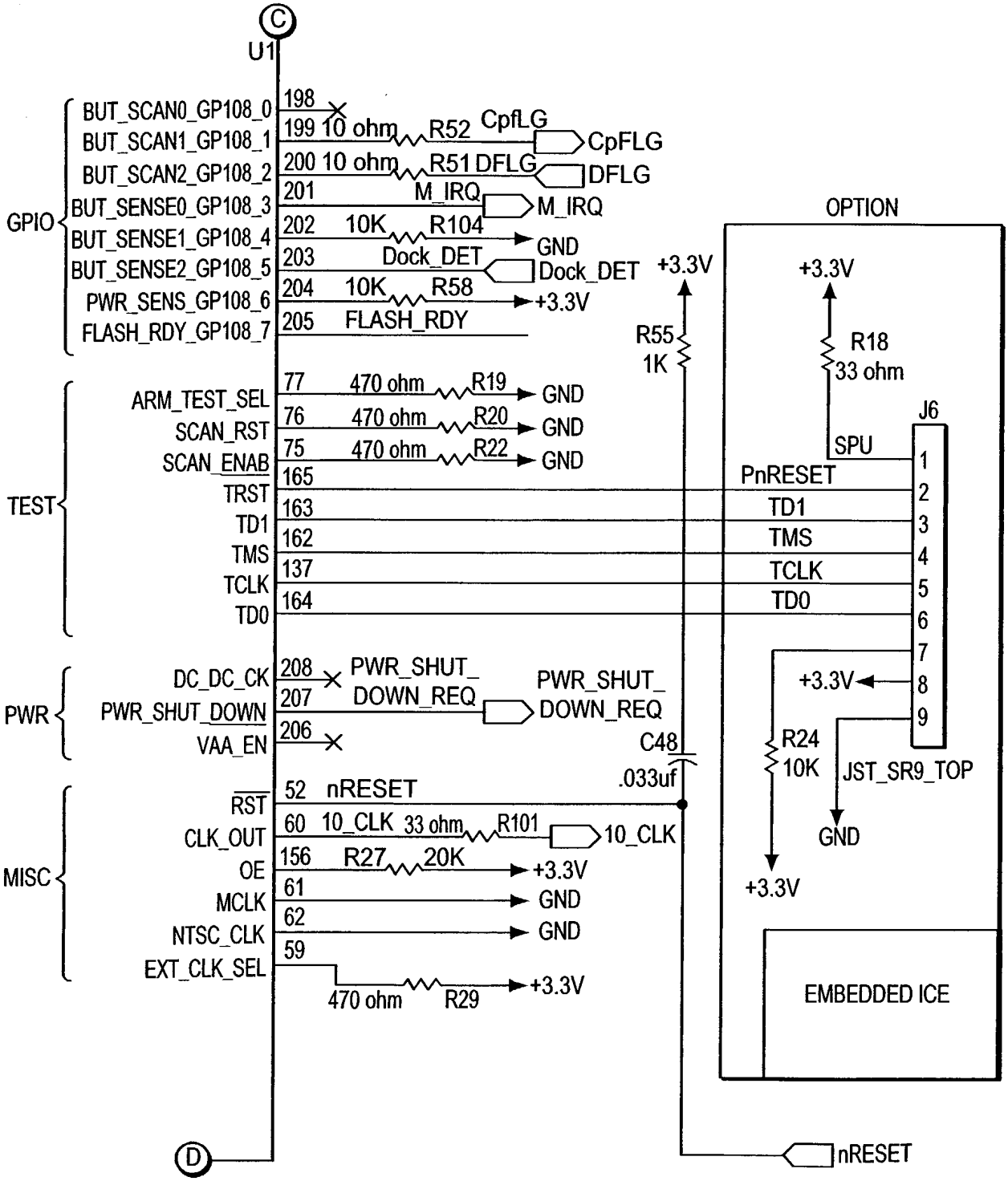

U1
GPIO
BUT_SCAN0_GP108_0
BUT_SCAN1_GP108_1
BUT_SCAN2_GP108_2
BUT_SENSE0_GP108_3
BUT_SENSE1_GP108_4
BUT_SENSE2_GP108_5
PWR_SENS_GP108_6
FLASH_RDY_GP108_7
198
199 10 ohm R52 CpfLG
200 10 ohm R51 DFLG
201 M_IRQ
202 10K R104
203 Dock_DET
204 10K R58
205 FLASH_RDY
CpFLG
DFLG
M_IRQ
GND
Dock_DET
+3.3V
TEST
ARM_TEST_SEL
SCAN_RST
SCAN_ENAB
TRST
TD1
TMS
TCLK
TD0
77 470 ohm R19
76 470 ohm R20
75 470 ohm R22
165
163
162
137
164
PWR
DC_DC_CK
PWR_SHUT_DOWN
VAA_EN
208
207
206
PWR_SHUT_ DOWN_REQ
PWR_SHUT_ DOWN_REQ
MISC
RST
CLK_OUT
OE
MCLK
NTSC_CLK
EXT_CLK_SEL
52 nRESET
60 10_CLK 33 ohm R101
156 R27 20K
61
62
59
470 ohm R29
10_CLK
+3.3V
GND
R55
1K
C48
.033uf
OPTION
+3.3V
R18
33 ohm
J6
SPU
PnRESET
TD1
TMS
TCLK
TD0
1
2
3
4
5
6
7
8
9
+3.3V
R24
10K
JST_SR9_TOP
GND
+3.3V
EMBEDDED ICE
nRESET

FIG. 5D

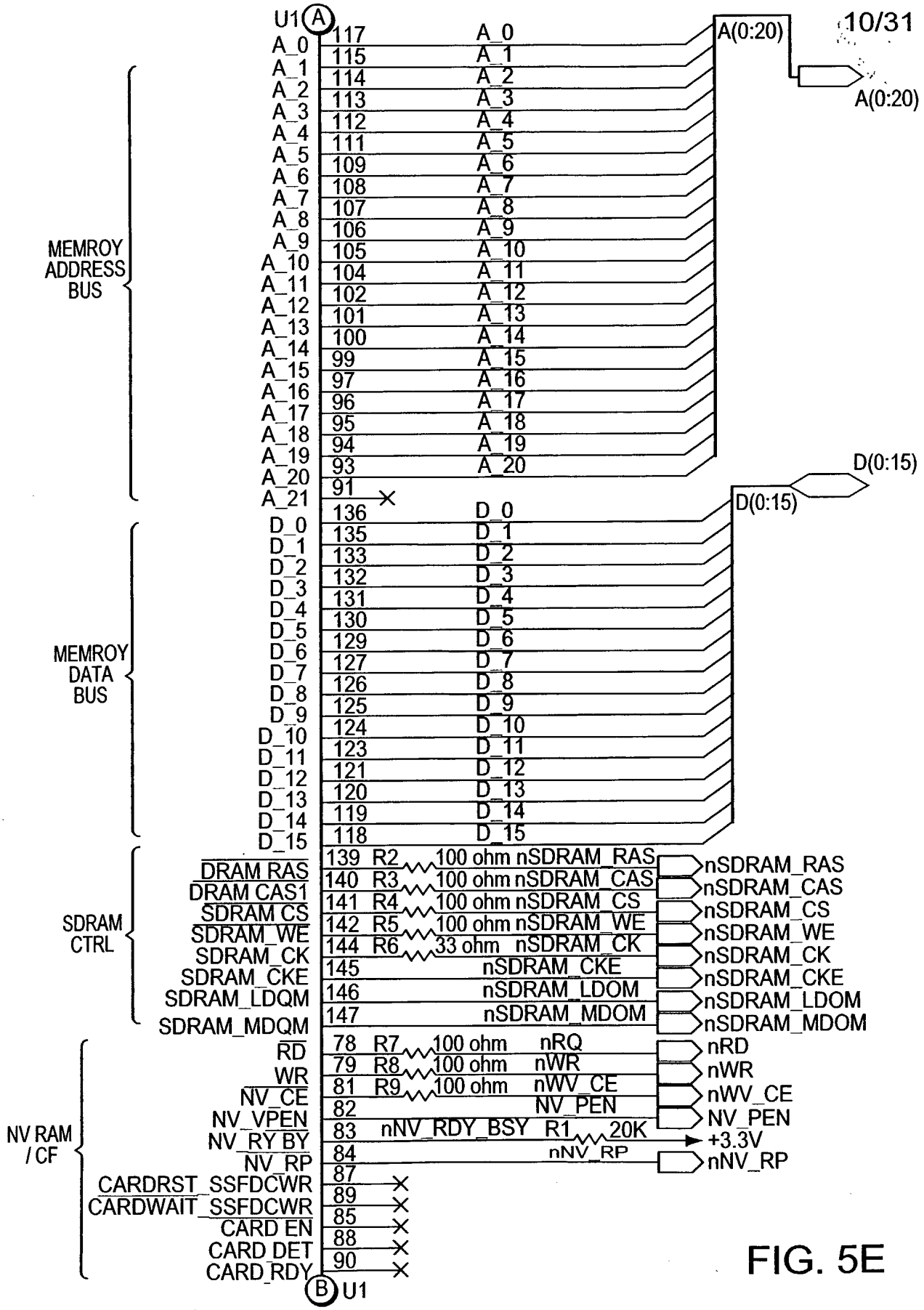

U1
A
MEMROY ADDRESS BUS
A_0 117 A_0
A_1 115 A_1
A_2 114 A_2
A_3 113 A_3
A_4 112 A_4
A_5 111 A_5
A_6 109 A_6
A_7 108 A_7
A_8 107 A_8
A_9 106 A_9
A_10 105 A_10
A_11 104 A_11
A_12 102 A_12
A_13 101 A_13
A_14 100 A_14
A_15 99 A_15
A_16 97 A_16
A_17 96 A_17
A_18 95 A_18
A_19 94 A_19
A_20 93 A_20
A_21 91
A(0:20)
A(0:20)
MEMROY DATA BUS
D_0 136 D_0
D_1 135 D_1
D_2 133 D_2
D_3 132 D_3
D_4 131 D_4
D_5 130 D_5
D_6 129 D_6
D_7 127 D_7
D_8 126 D_8
D_9 125 D_9
D_10 124 D_10
D_11 123 D_11
D_12 121 D_12
D_13 120 D_13
D_14 119 D_14
D_15 118 D_15
D(0:15)
D(0:15)
SDRAM CTRL
DRAM RAS 139 R2 100 ohm nSDRAM_RAS nSDRAM_RAS
DRAM CAS1 140 R3 100 ohm nSDRAM_CAS nSDRAM_CAS
SDRAM CS 141 R4 100 ohm nSDRAM_CS nSDRAM_CS
SDRAM_WE 142 R5 100 ohm nSDRAM_WE nSDRAM_WE
SDRAM_CK 144 R6 33 ohm nSDRAM_CK nSDRAM_CK
SDRAM_CKE 145 nSDRAM_CKE nSDRAM_CKE
SDRAM_LDQM 146 nSDRAM_LDOM nSDRAM_LDOM
SDRAM_MDQM 147 nSDRAM_MDOM nSDRAM_MDOM
NV RAM / CF
RD 78 R7 100 ohm nRQ nRD
WR 79 R8 100 ohm nWR nWR
NV_CE 81 R9 100 ohm nWV_CE nWV_CE
NV_VPEN 82 NV_PEN NV_PEN
NV_RY BY 83 nNV_RDY_BSY R1 20K +3.3V
NV_RP 84 nNV_RP nNV_RP
CARDRST_SSFDCWR 87
CARDWAIT_SSFDCWR 89
CARD EN 85
CARD DET 88
CARD_RDY 90
B
U1

FIG. 5E

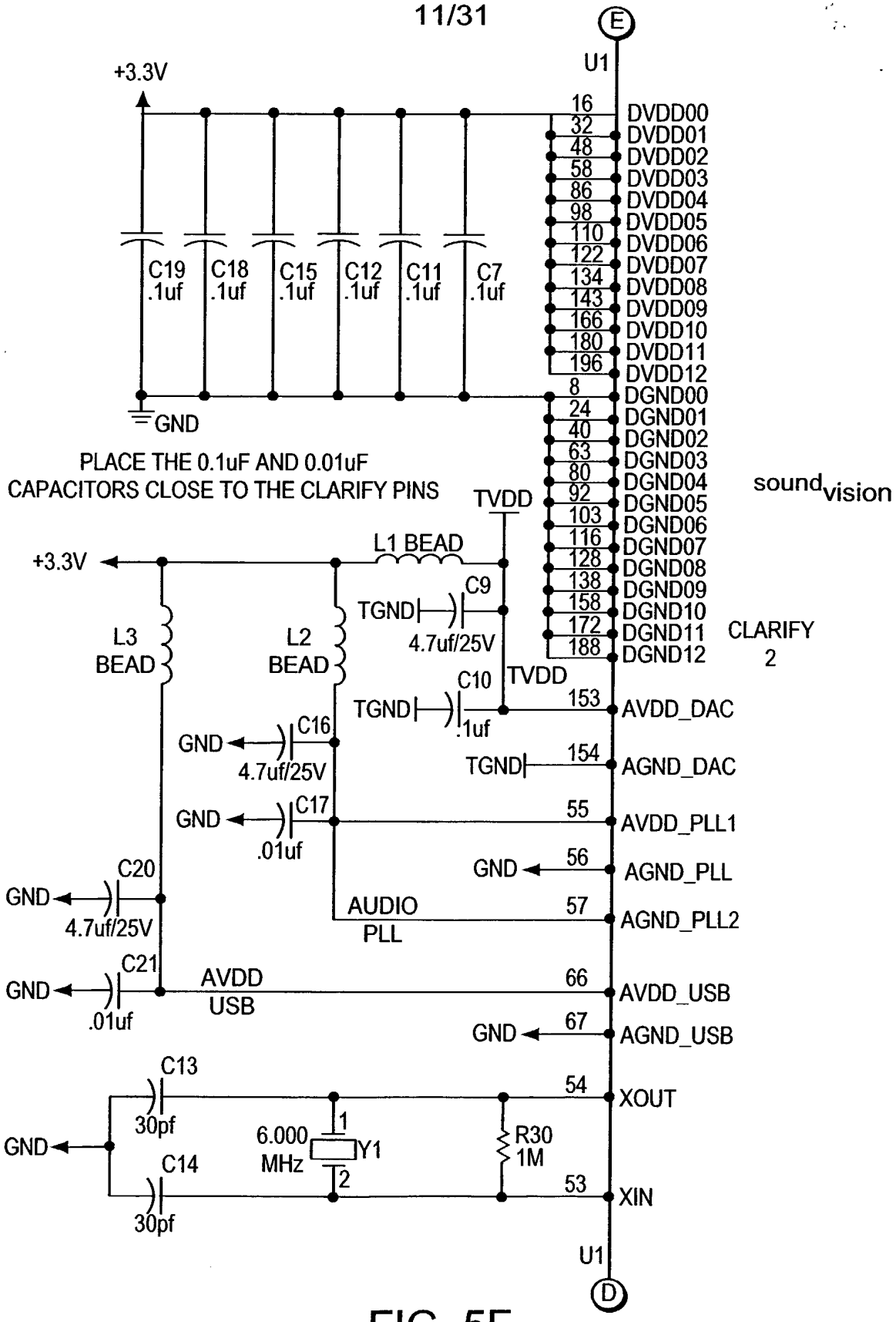
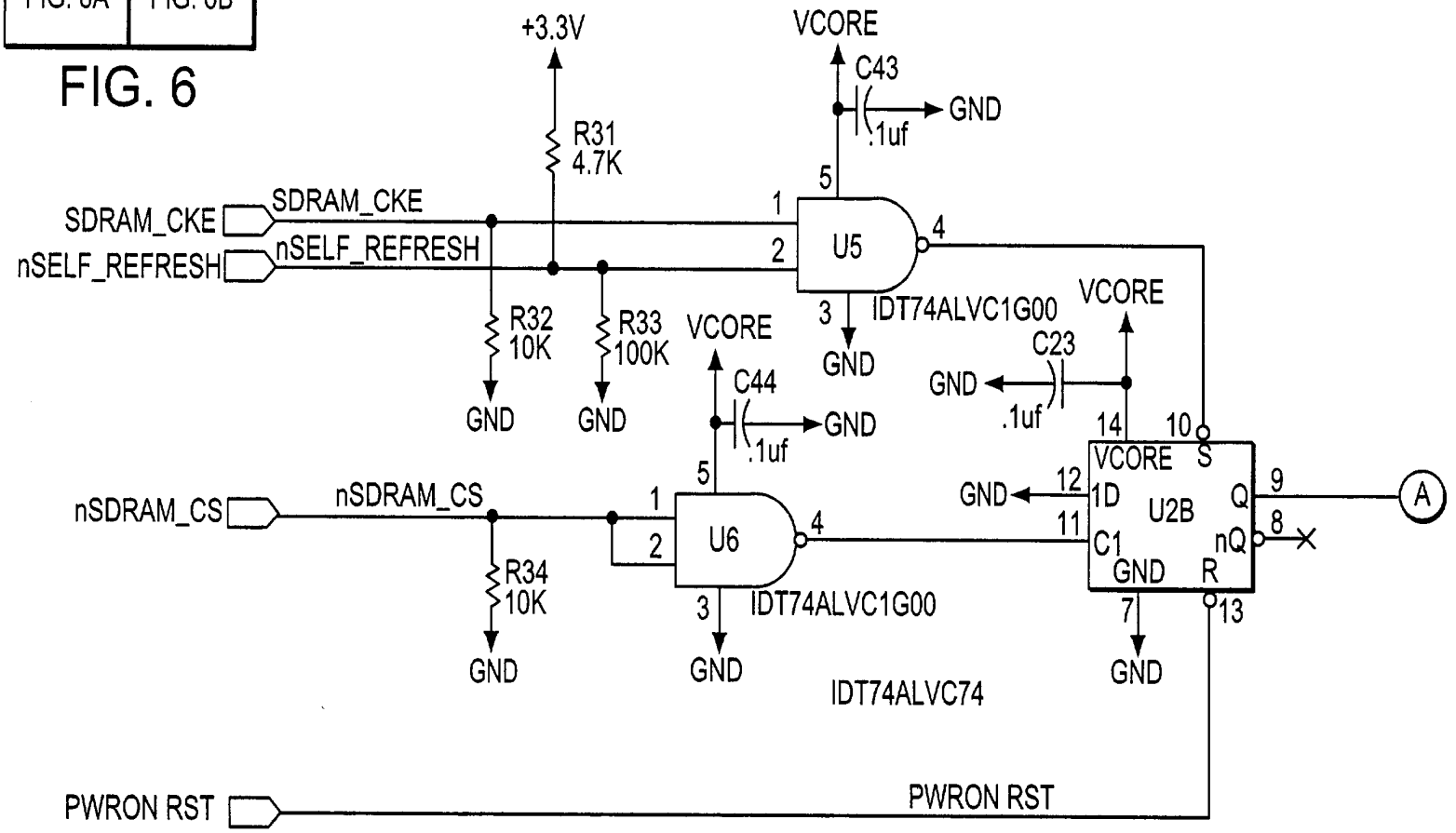

E
U1
+3.3V
16 DVDD00
32 DVDD01
48 DVDD02
58 DVDD03
86 DVDD04
98 DVDD05
110 DVDD06
122 DVDD07
134 DVDD08
143 DVDD09
166 DVDD10
180 DVDD11
196 DVDD12
8 DGND00
24 DGND01
40 DGND02
63 DGND03
80 DGND04
92 DGND05
103 DGND06
116 DGND07
128 DGND08
138 DGND09
158 DGND10
172 DGND11
188 DGND12
C19 .1uf
C18 .1uf
C15 .1uf
C12 .1uf
C11 .1uf
C7 .1uf
GND
PLACE THE 0.1uF AND 0.01uF CAPACITORS CLOSE TO THE CLARIFY PINS
TVDD
L1 BEAD
+3.3V
C9
TGND
4.7uf/25V
L3 BEAD
L2 BEAD
C10
TVDD
TGND
.1uf
153 AVDD_DAC
C16
GND
4.7uf/25V
TGND
154 AGND_DAC
C17
GND
.01uf
55 AVDD_PLL1
GND
56 AGND_PLL
C20
GND
4.7uf/25V
AUDIO PLL
57 AGND_PLL2
C21
GND
.01uf
AVDD USB
66 AVDD_USB
GND
67 AGND_USB
C13
30pf
54 XOUT
GND
6.000 MHz
1
2
Y1
R30 1M
C14
30pf
53 XIN
U1
D
sound vision
CLARIFY 2

FIG. 5F

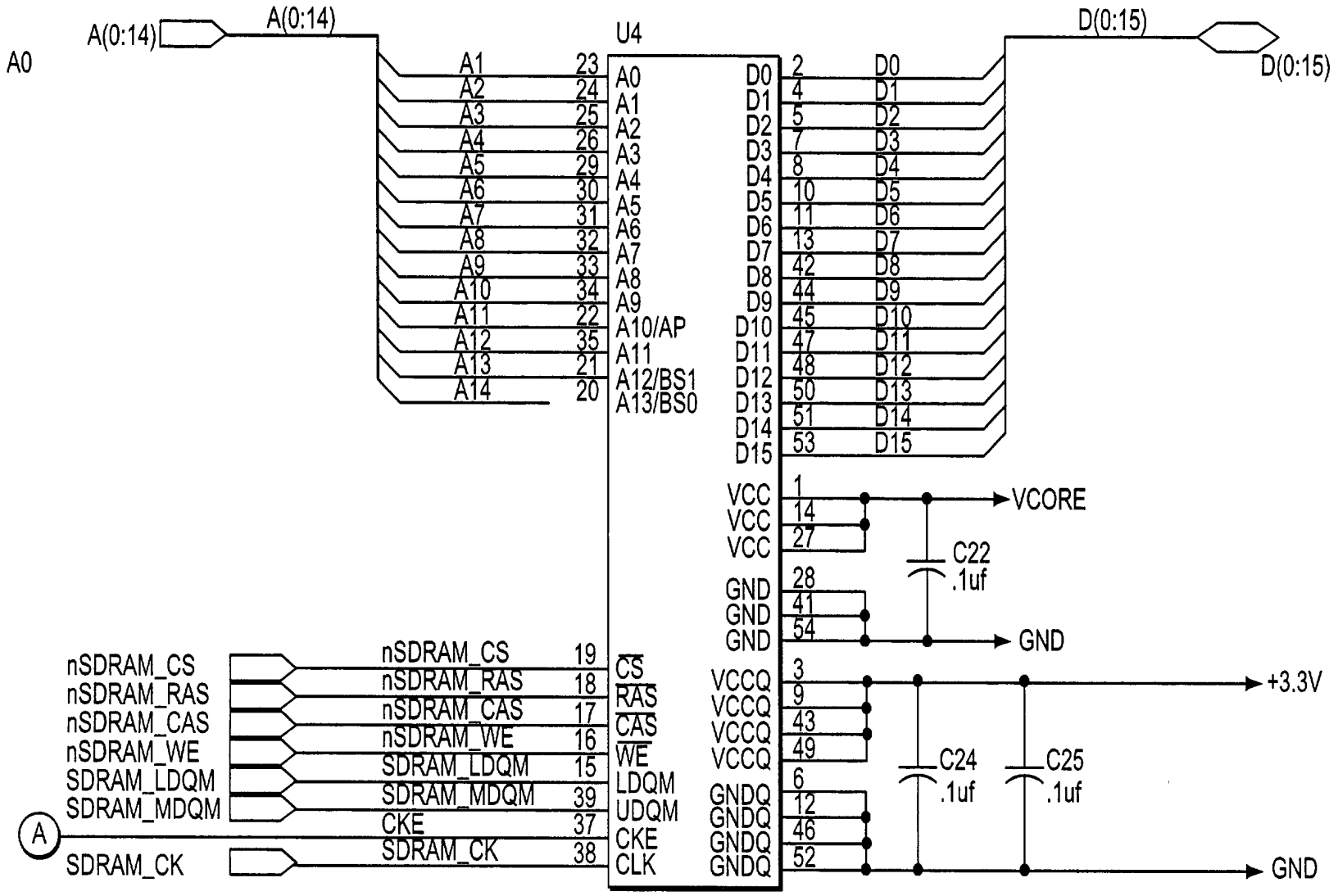
FIG. 6A	FIG. 6B

FIG. 6



LOW POWER SDRAM SHOULD BE USED. POWER CONSUMPTION WHEN THE CAMERA IS SHUT DOWN DEPENDS ON THE SDRAM CONSUMPTION IN SELF REFRESH MODE AS THE MAJOR COMPONENT OF QUIESCENT CONSUMPTION.

FIG. 6A



SDRAM 4 MEG x 16 - LOW POWER

13/31

FIG. 6B

4M x 16 SDRAM SHOWN, CAN ALSO USE
1M x 16 WITHIN THE SAME FOOTPRINT.

NOTE: THIS DESIGN REQUIRES SDRAM PARTS
WITH ISOLATED Vcc AND VccQ ON CHIP.

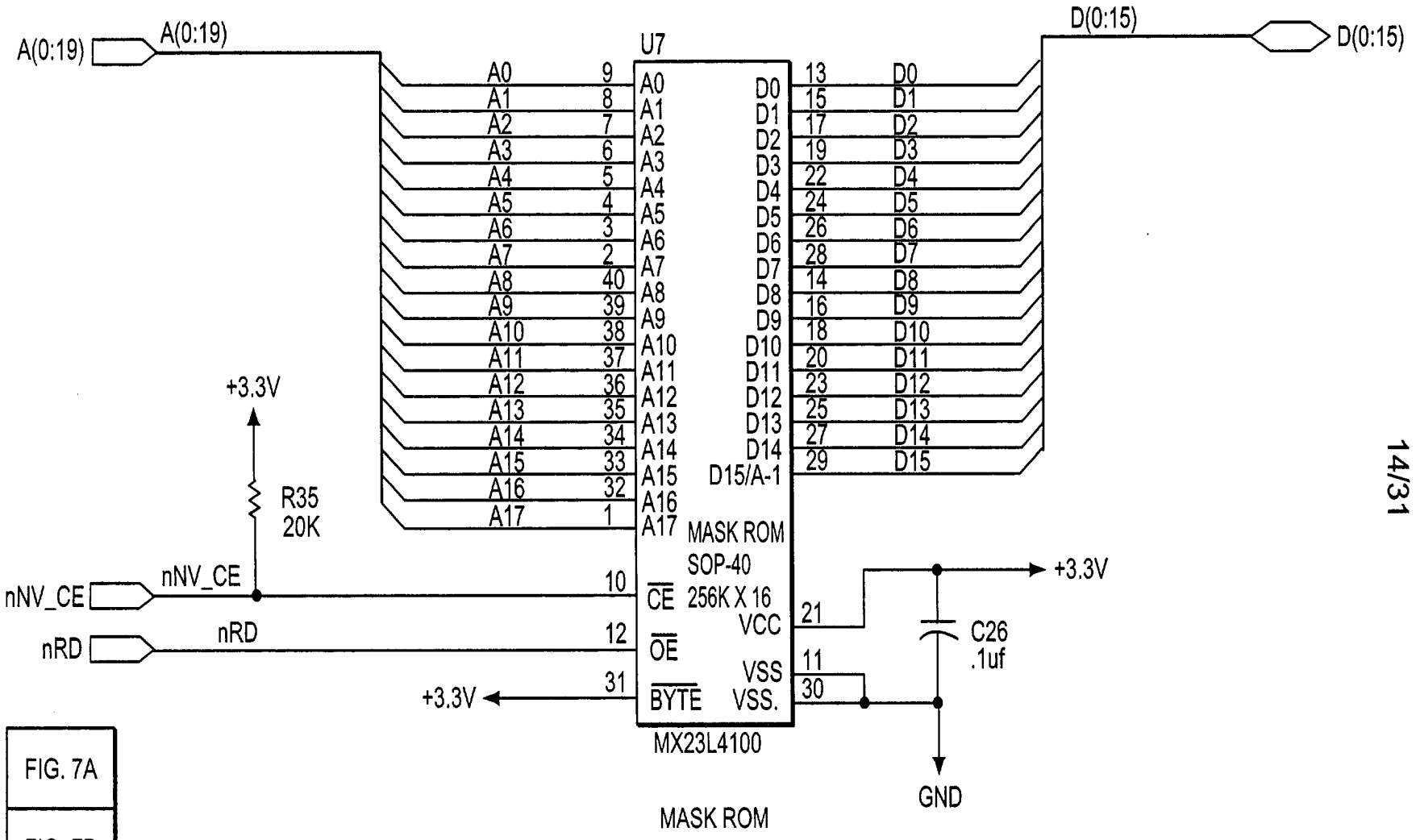


FIG. 7A

FIG. 7A
FIG. 7B

FIG. 7

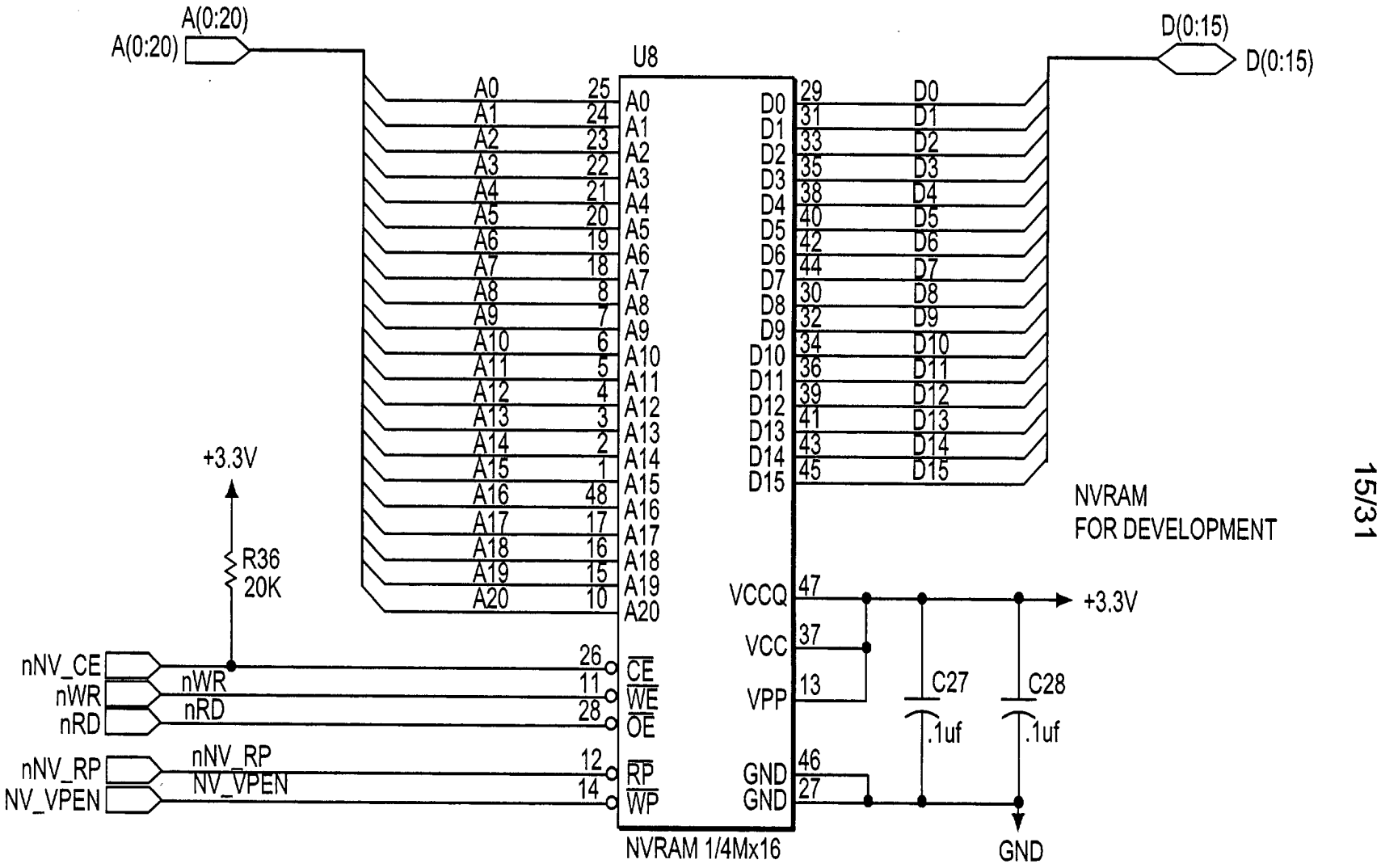

A(0:20)
A(0:20)
U8
D(0:15)
D(0:15)
A0 25
A1 24
A2 23
A3 22
A4 21
A5 20
A6 19
A7 18
A8 8
A9 7
A10 6
A11 5
A12 4
A13 3
A14 2
A15 1
A16 48
A17 17
A18 16
A19 15
A20 10
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
D0 29
D1 31
D2 33
D3 35
D4 38
D5 40
D6 42
D7 44
D8 30
D9 32
D10 34
D11 36
D12 39
D13 41
D14 43
D15 45
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
NVRAM
FOR DEVELOPMENT
+3.3V
R36
20K
nNV_CE
nWR
nRD
nNV_RP
NV_VPEN
26 CE
11 WE
28 OE
12 RP
14 WP
VCCQ 47
VCC 37
VPP 13
GND 46
GND 27
+3.3V
C27
.1uf
C28
.1uf
GND
NVRAM 1/4Mx16

FIG. 7B

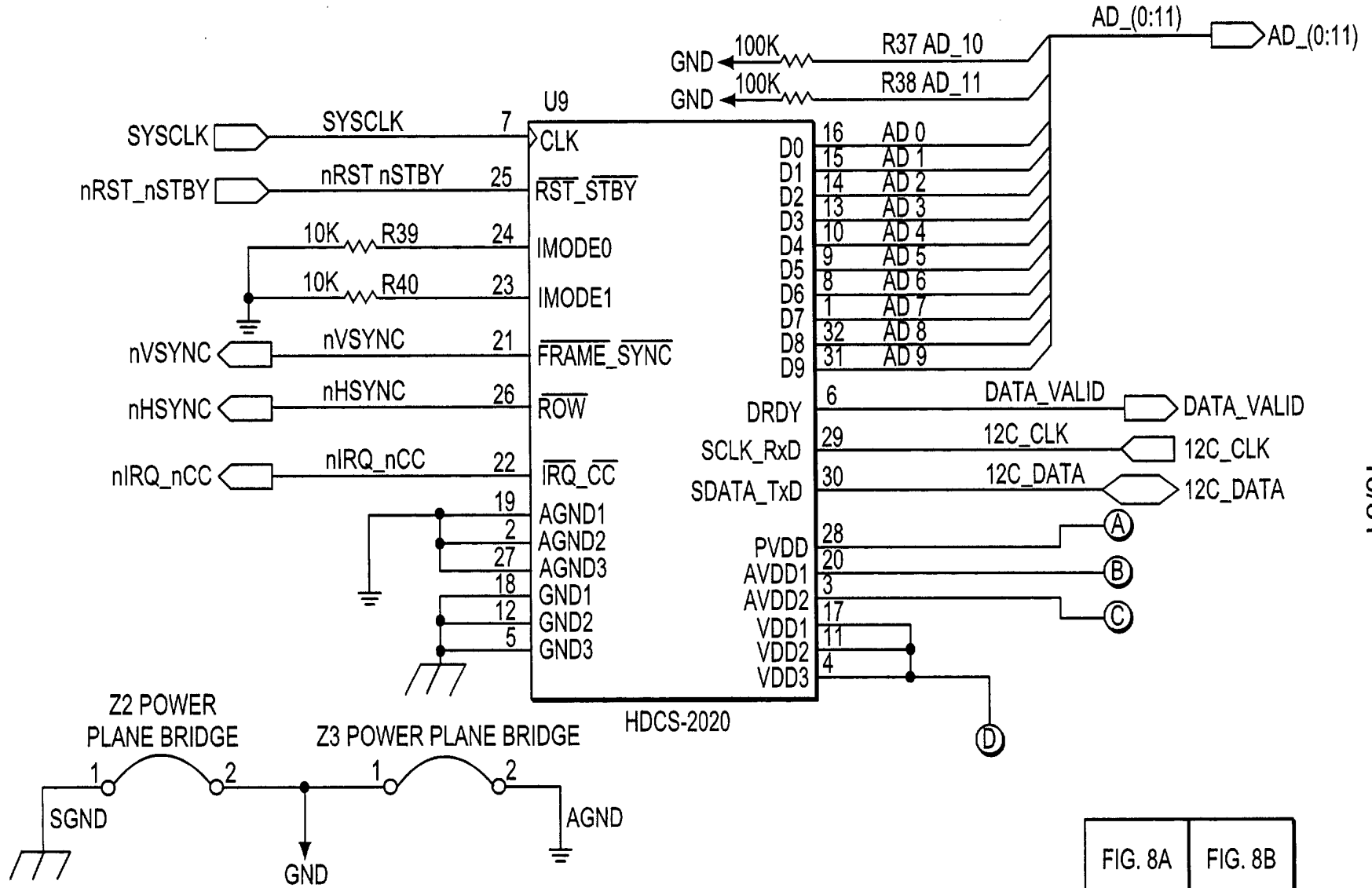


FIG. 8A

FIG. 8A | FIG. 8B

FIG. 8

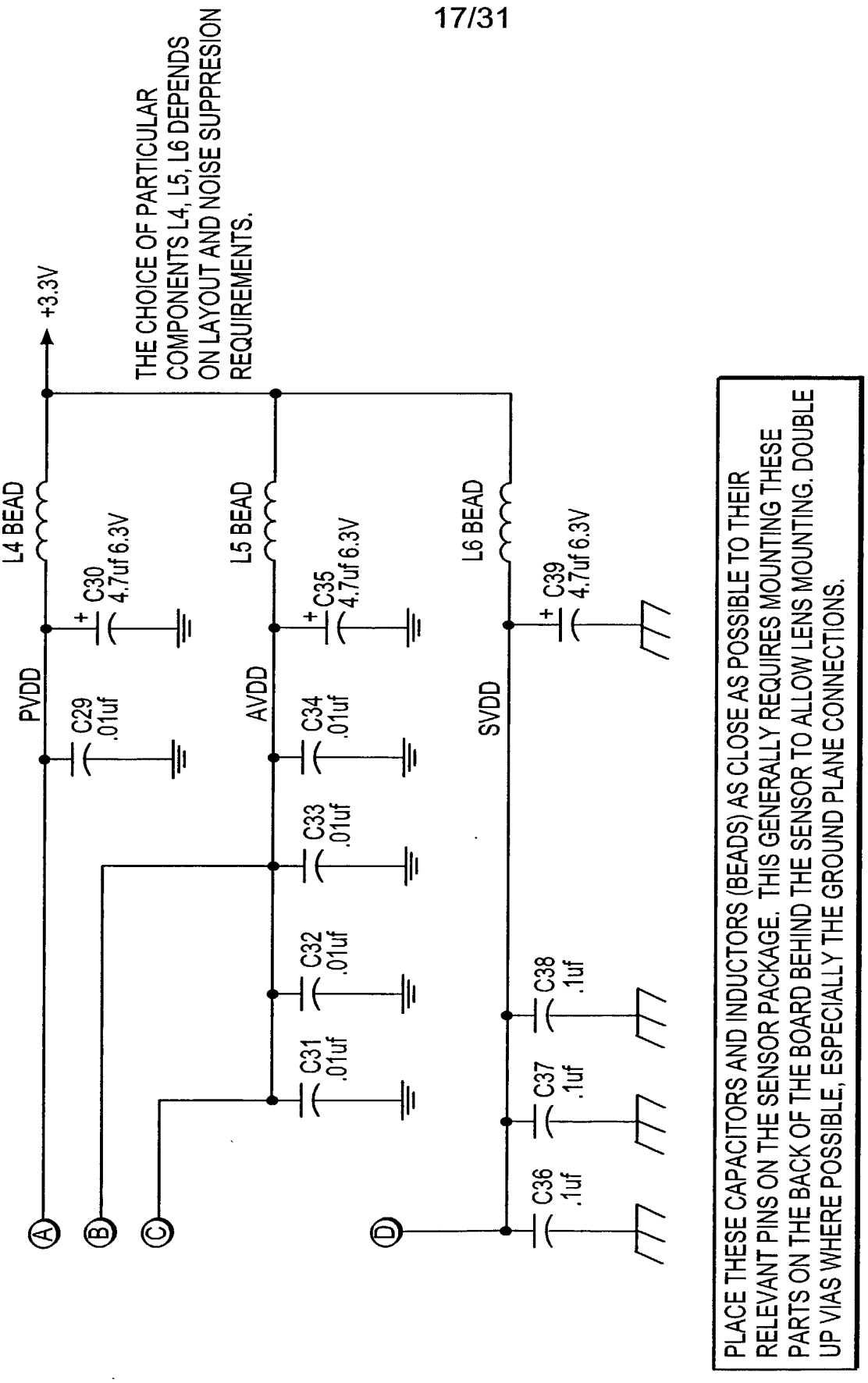
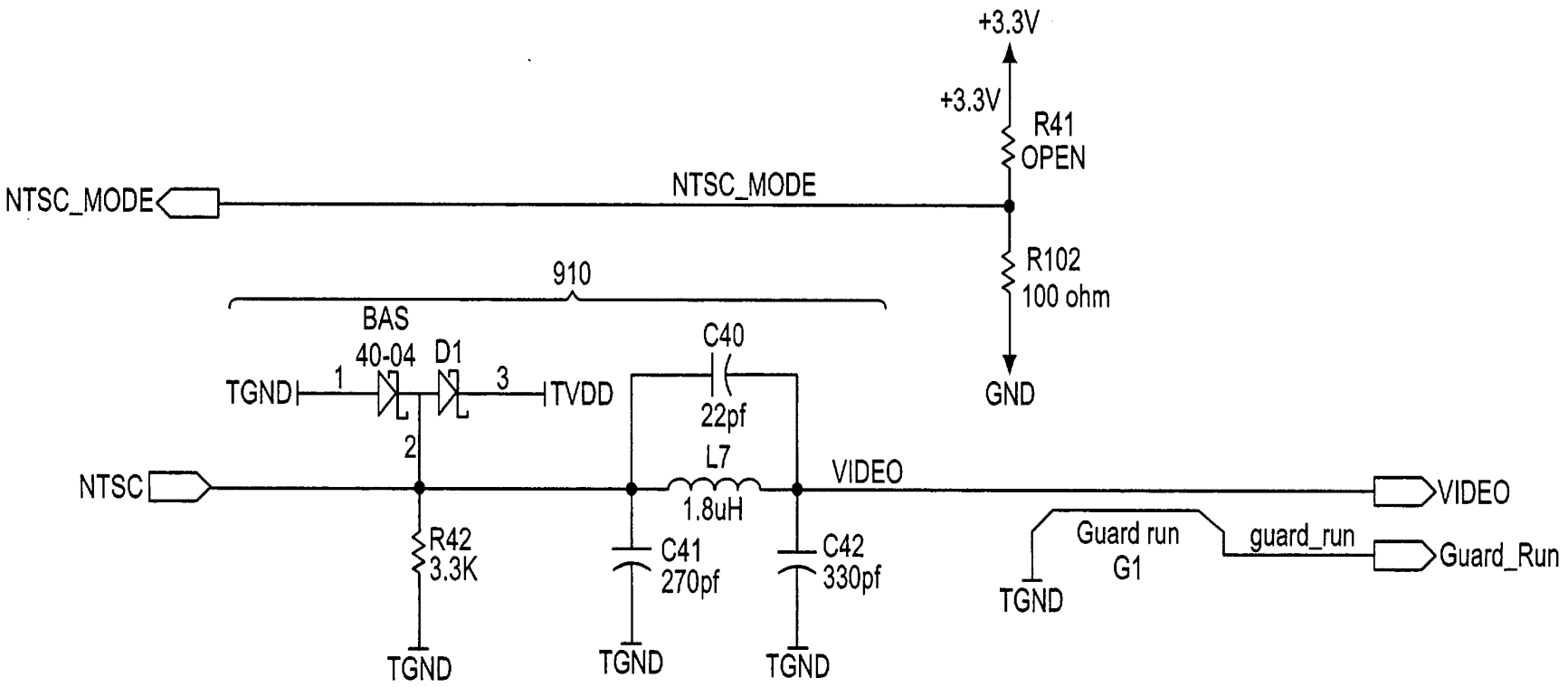
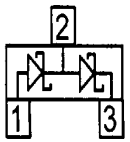

+3.3V
THE CHOICE OF PARTICULAR COMPONENTS L4, L5, L6 DEPENDS ON LAYOUT AND NOISE SUPPRESION REQUIREMENTS.
L4 BEAD
L5 BEAD
L6 BEAD
PVDD
AVDD
SVDD
C29 .01uf
C30 4.7uf 6.3V
C31 .01uf
C32 .01uf
C33 .01uf
C34 .01uf
C35 4.7uf 6.3V
C36 .1uf
C37 .1uf
C38 .1uf
C39 4.7uf 6.3V
A
B
C
D
PLACE THESE CAPACITORS AND INDUCTORS (BEADS) AS CLOSE AS POSSIBLE TO THEIR RELEVANT PINS ON THE SENSOR PACKAGE. THIS GENERALLY REQUIRES MOUNTING THESE PARTS ON THE BACK OF THE BOARD BEHIND THE SENSOR TO ALLOW LENS MOUNTING. DOUBLE UP VIAS WHERE POSSIBLE, ESPECIALLY THE GROUND PLANE CONNECTIONS.

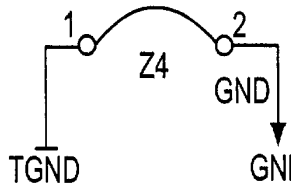
FIG. 8B



NOTE:
THE DIODE PIN NUMBERING SHOWN HERE IS NON-STANDARD. MAKE SURE THE PCB LAYOUT MATCHES THE DIODE(S) USED IN YOUR DESIGN.



POWER PLANE BRIDGE



TGND IS A PORTION OF THE GROUND PLANE PROTECTED WITH CUTS. SEE CLARITY SHEET. IT IS NOT A SEPARATE RUN!

FIG. 9

FIG. 10A	FIG. 10B

FIG. 10

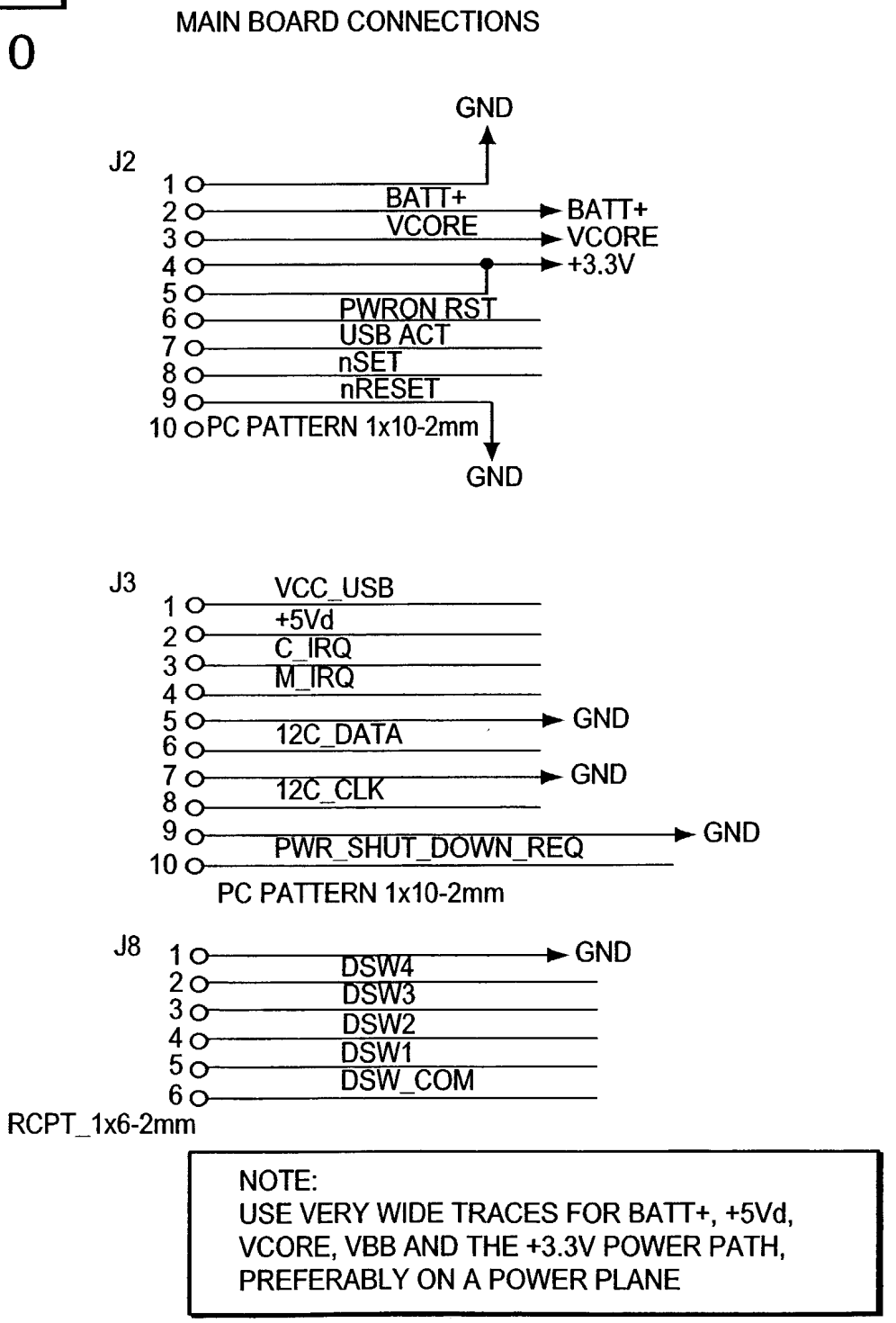


FIG. 10A

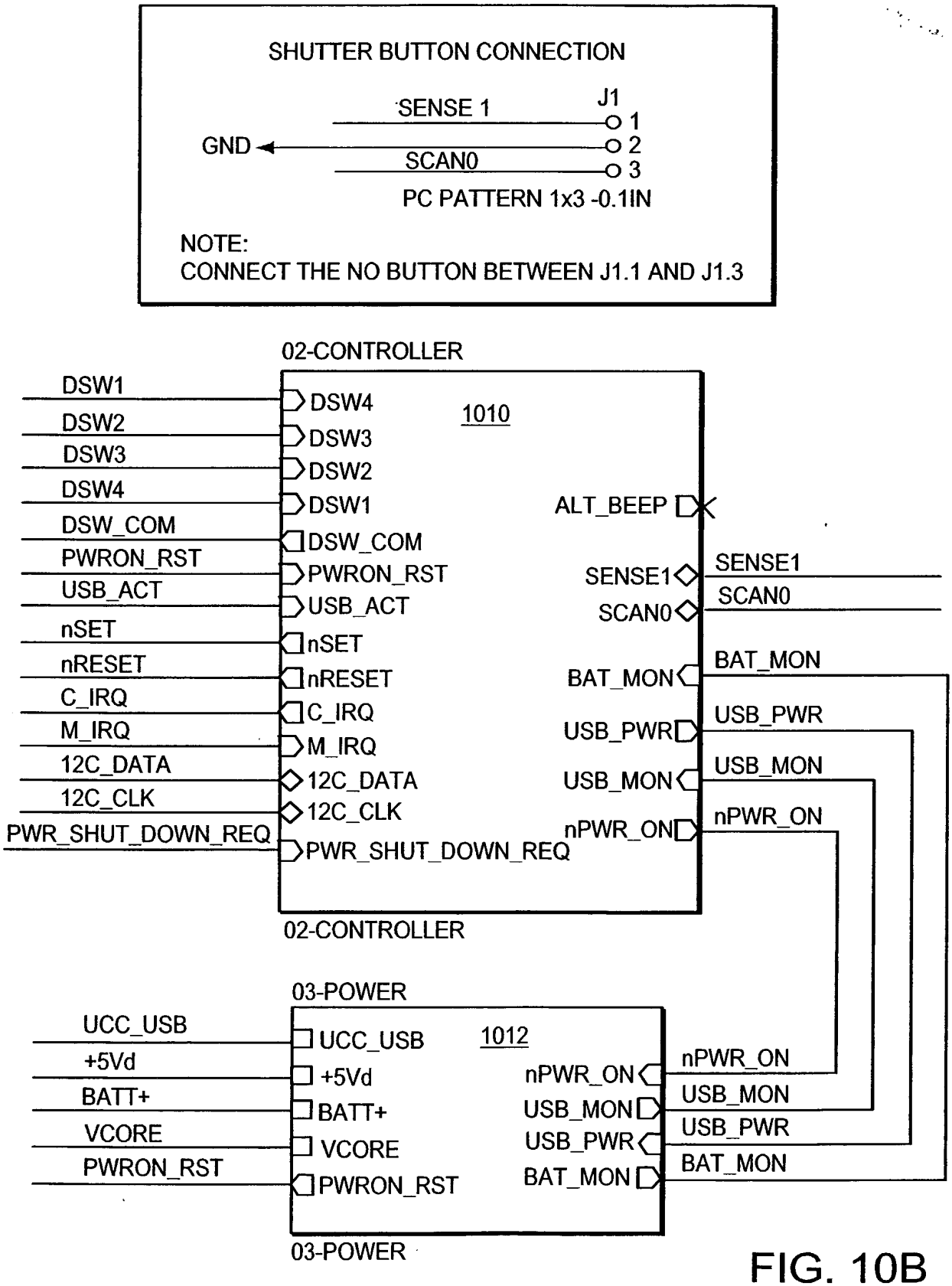

SHUTTER BUTTON CONNECTION
SENSE 1
J1
1
GND
2
SCAN0
3
PC PATTERN 1x3 -0.1IN
NOTE:
CONNECT THE NO BUTTON BETWEEN J1.1 AND J1.3
02-CONTROLLER
1010
DSW1
DSW2
DSW3
DSW4
DSW_COM
PWRON_RST
USB_ACT
nSET
nRESET
C_IRQ
M_IRQ
12C_DATA
12C_CLK
PWR_SHUT_DOWN_REQ
ALT_BEEP
SENSE1
SCAN0
BAT_MON
USB_PWR
USB_MON
nPWR_ON
02-CONTROLLER
03-POWER
1012
UCC_USB
+5Vd
BATT+
VCORE
PWRON_RST
03-POWER

FIG. 10B

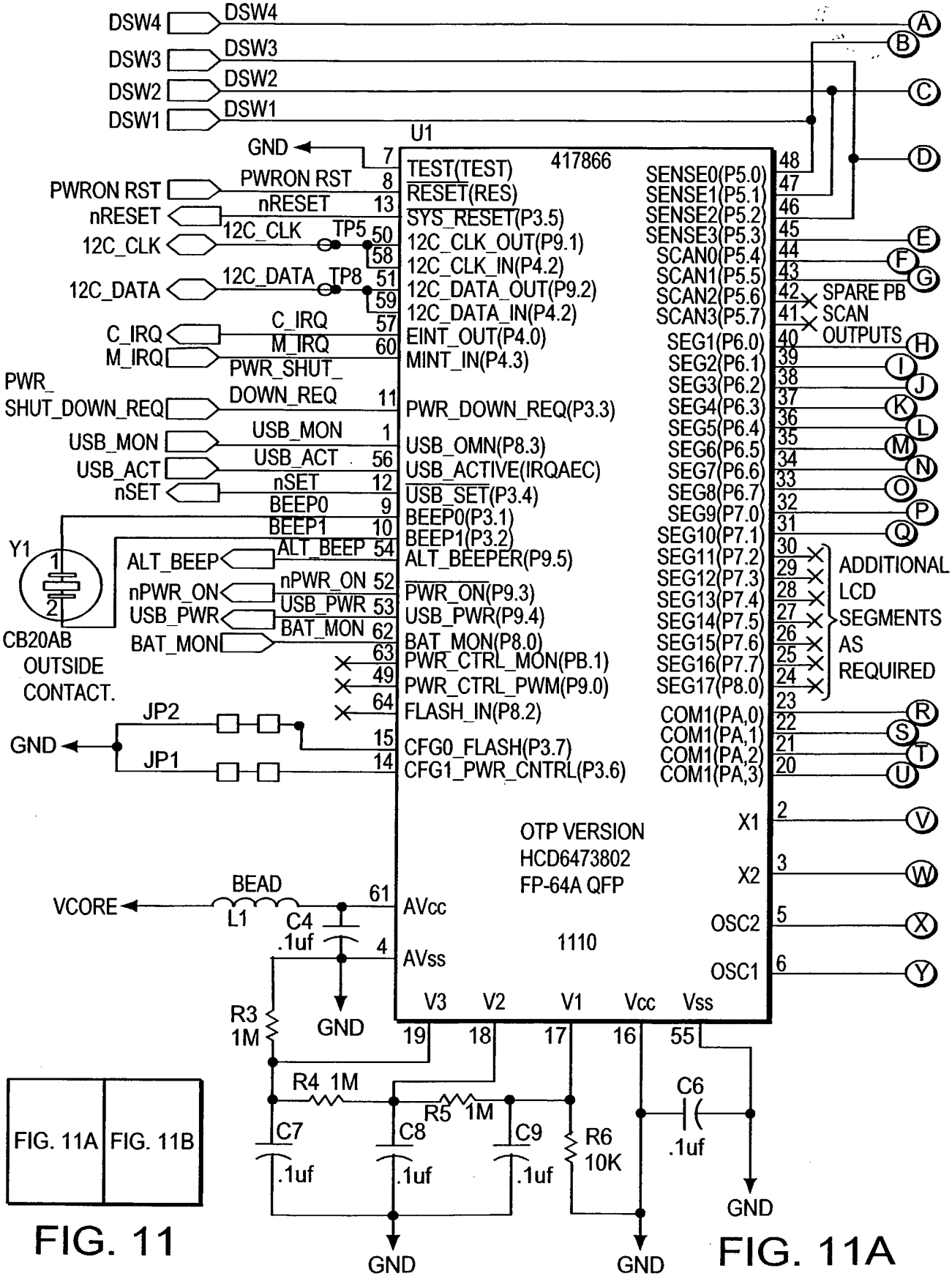
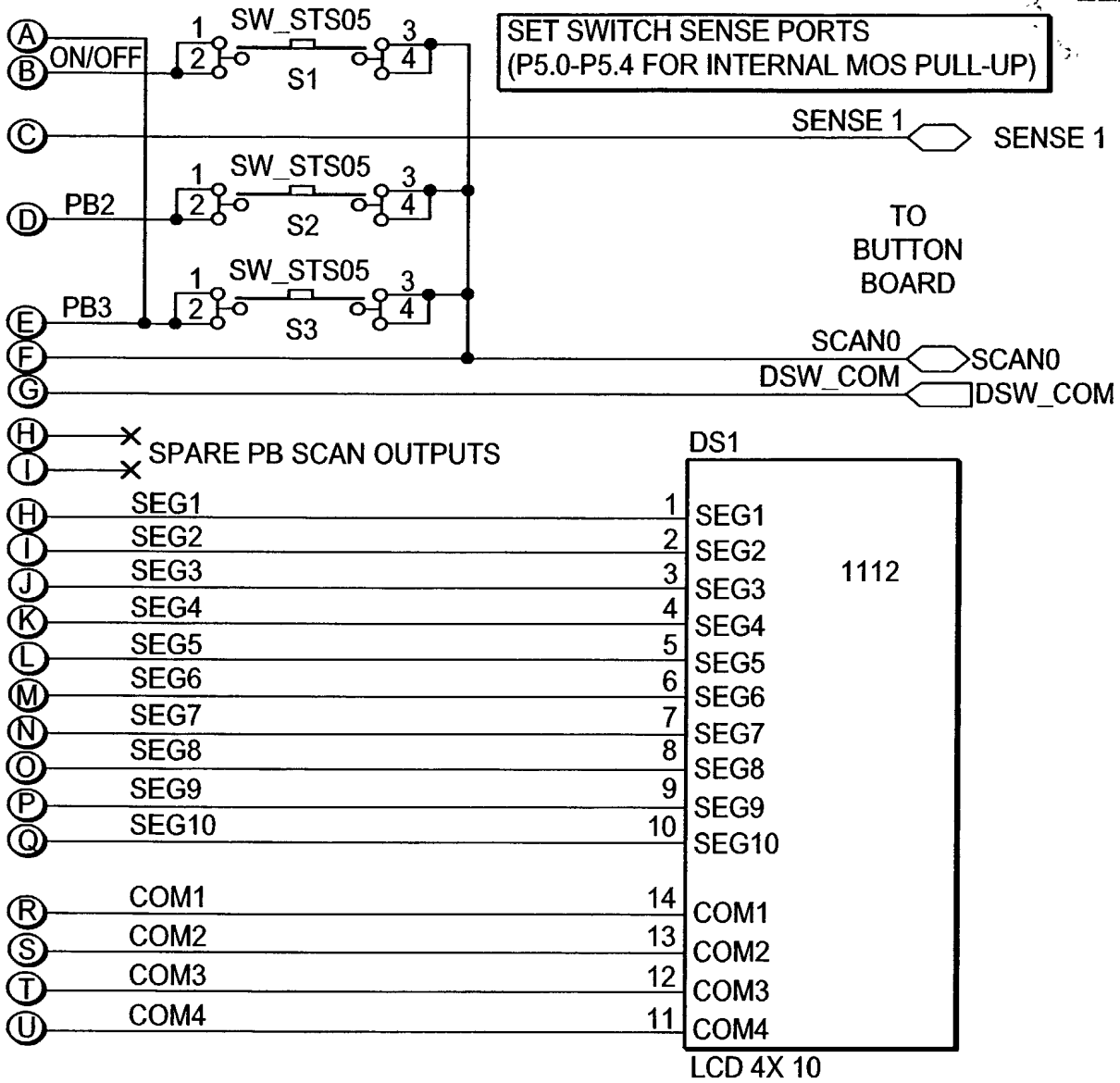
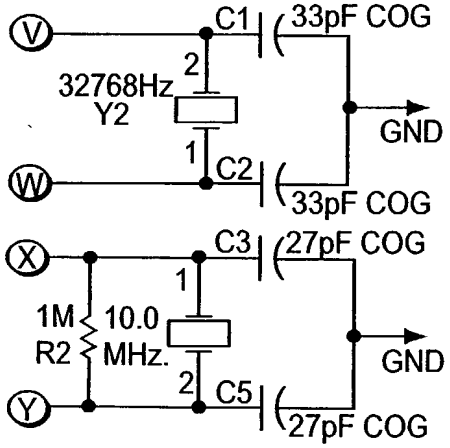


FIG. 11A FIG. 11B

FIG. 11

FIG. 11A





NOTES:
1. SET UNUSED PORT PINS TO OUTPUT LOW.
2. VCORE IS USED AS THE ADC REFERENCE BY THE CONTROLLER.
3. KEEP CRYSTAL AND RESONATOR CLOSE TO THE IC, SEE DATA SHEET.
4. USE THE INTEGRAL PULL UP IN THE SWITCH PORTS.
5. ON STARTUP USE P3.4 TO SET THE USB_ACT FLIP-FLOP BEFORE ENABLING THE IRQ TO SENSE USB DATA ACTIVITY.
6. THE H8/3802 IC SHOWN IS THE OTP VERSION FOR DEVELOPMENT ONLY. FOR PRODUCTION USE THE MASK ROM VERSION, HD6433800H OR THE LOWEST COST COB VERSION; HCD6433800-(***).
7. SET PORT 9 TO HIGH CURRENT MODE.

FIG. 11B

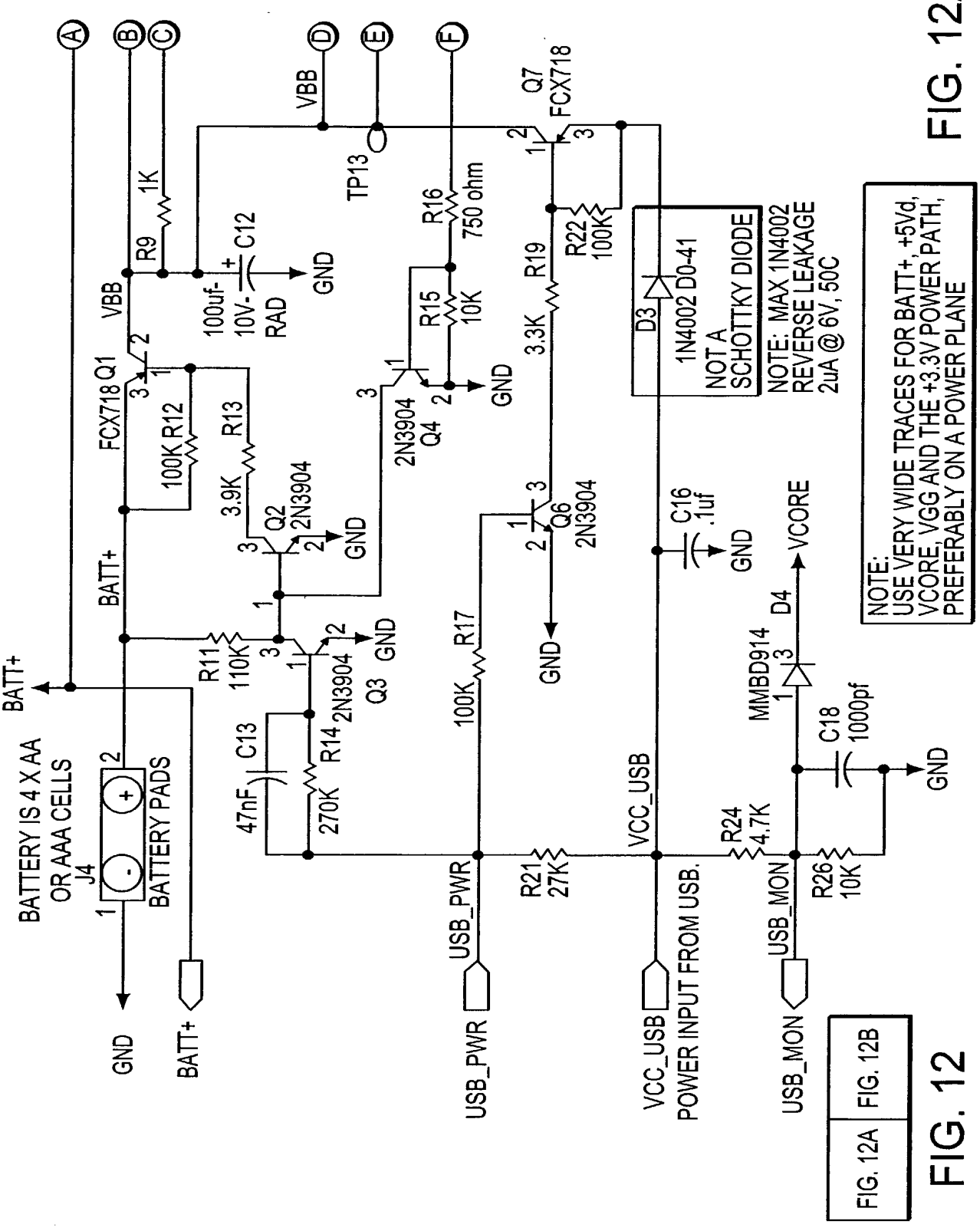

BATTERY IS 4 X AA
OR AAA CELLS
J4
BATTERY PADS
BATT+
GND
BATT+
R9 1K
VBB
100uf-
10V-
RAD
C12
GND
TP13
VBB
R16
750 ohm
R15
10K
GND
2N3904
Q4
R19
3.3K
Q7
FCX718
R22
100K
D3
1N4002 DO-41
NOT A
SCHOTTKY DIODE
NOTE: MAX 1N4002
REVERSE LEAKAGE
2uA @ 6V, 50C
FCX718 Q1
100K R12
R13
3.9K
Q2
2N3904
GND
R11
110K
Q3
2N3904
GND
C13
47nF
R14
270K
R17
100K
Q6
2N3904
GND
C16
.1uf
GND
VCORE
D4
MMBD914
C18
1000pf
GND
USB_PWR
R21
27K
VCC_USB
R24
4.7K
USB_MON
R26
10K
USB_PWR
VCC_USB
POWER INPUT FROM USB.
USB_MON
NOTE:
USE VERY WIDE TRACES FOR BATT+, +5Vd,
VCORE, VGG AND THE +3.3V POWER PATH,
PREFERABLY ON A POWER PLANE
FIG. 12A
FIG. 12B

FIG. 12

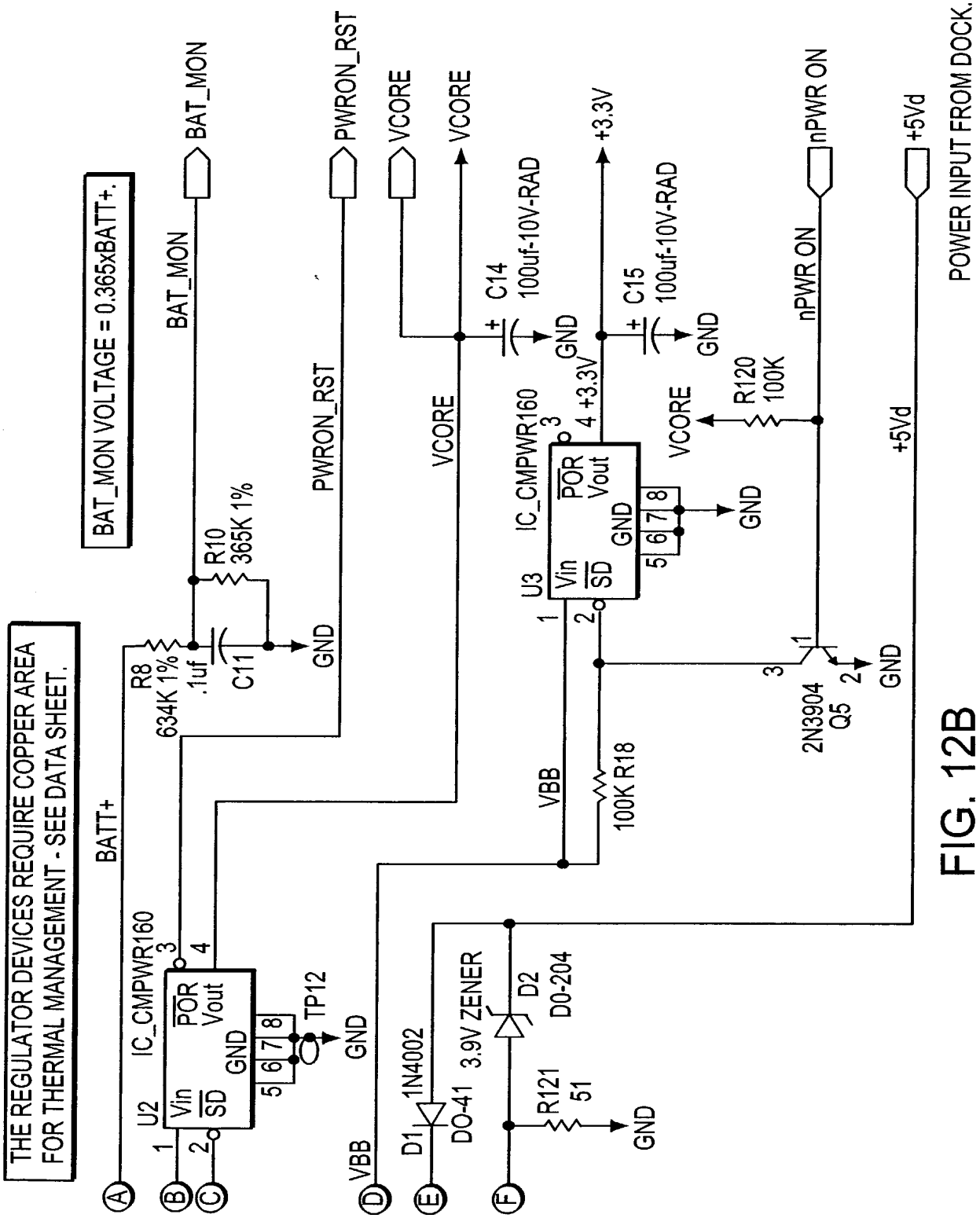
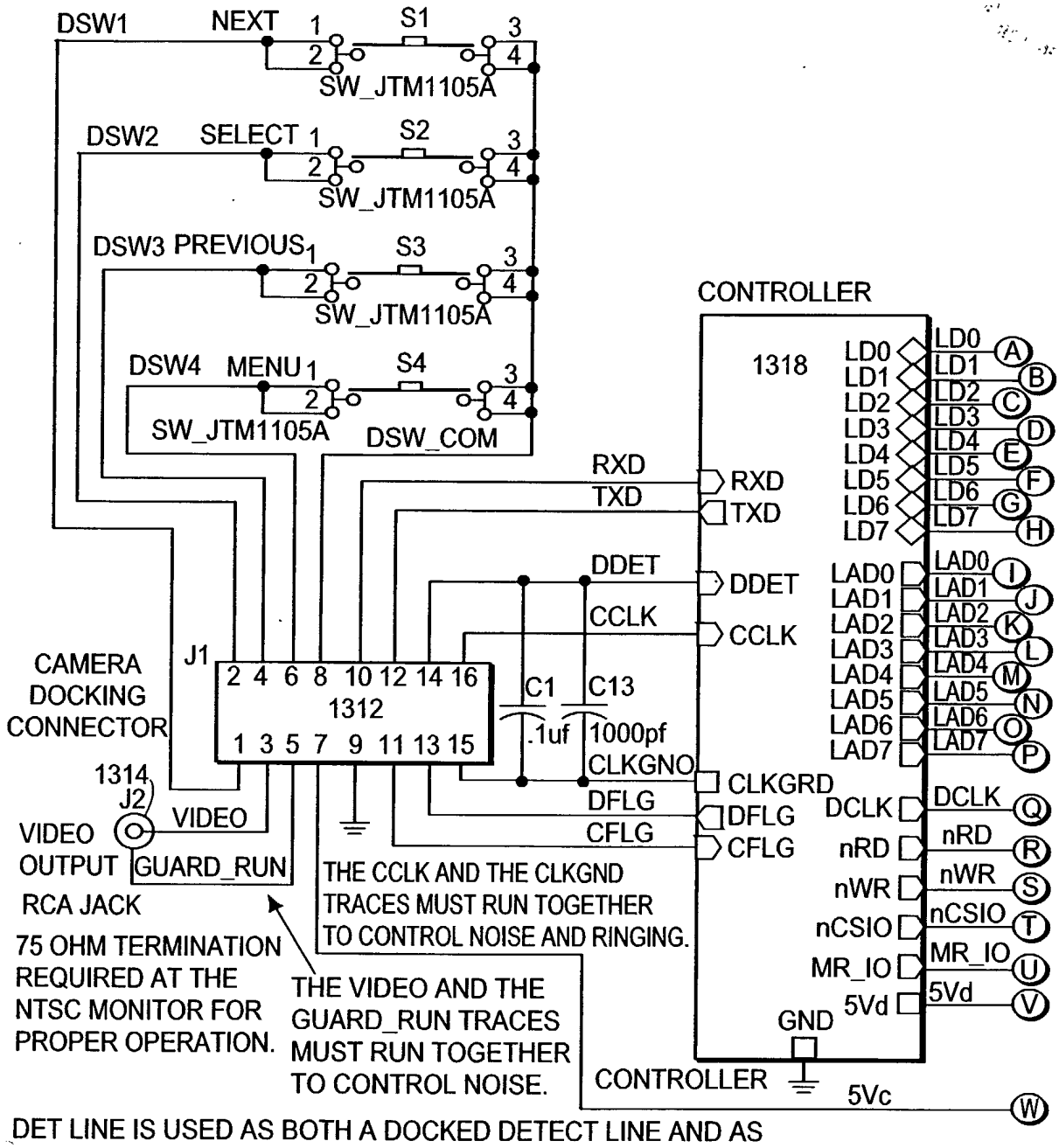

THE REGULATOR DEVICES REQUIRE COPPER AREA FOR THERMAL MANAGEMENT - SEE DATA SHEET.
BAT_MON VOLTAGE = 0.365xBATT+.
BAT_MON
PWRON_RST
VCORE
VCORE
+3.3V
nPWR ON
nPWR ON
+5Vd
POWER INPUT FROM DOCK.
BATT+
R8 634K 1%
.1uf
C11
R10 365K 1%
GND
PWRON_RST
VCORE
C14 100uf-10V-RAD
GND
C15 100uf-10V-RAD
GND
U2 IC_CMPWR160
Vin
SD
POR
Vout
GND
TP12
GND
U3 IC_CMPWR160
+3.3V
VCORE
R120 100K
GND
VBB
100K R18
2N3904 Q5
GND
VBB
D1 1N4002 DO-41
D2 3.9V ZENER DO-204
R121 51
GND
A
B
C
D
E
F

FIG. 12B



DET LINE IS USED AS BOTH A DOCKED DETECT LINE AND AS PART OF THE CLOCK BALANCING. MOUNT THE BYPASS CAPACITORS CLOSE TO THE BASE RESISTOR FOR THE RESET TRANSISTOR, Q1, ON THE CONTROLLER PAGE.

FIG. 13A	FIG. 13B

FIG. 13

FIG. 13A

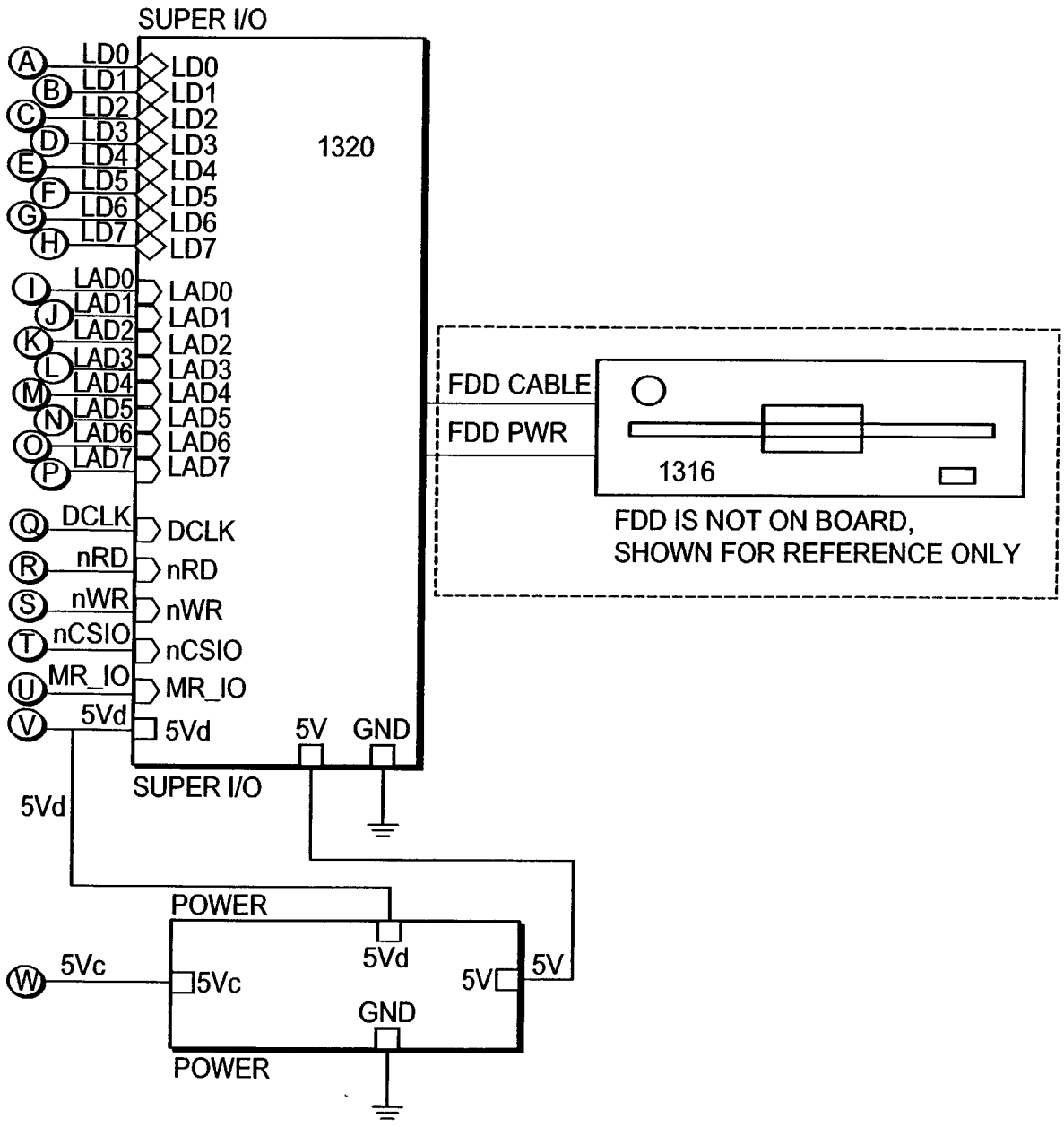

1310
SUPER I/O
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
1320
LAD0
LAD1
LAD2
LAD3
LAD4
LAD5
LAD6
LAD7
DCLK
nRD
nWR
nCSIO
MR_IO
5Vd
5V
GND
SUPER I/O
FDD CABLE
FDD PWR
1316
FDD IS NOT ON BOARD,
SHOWN FOR REFERENCE ONLY
5Vd
POWER
5Vc
5Vd
5V
GND
POWER

FIG. 13B

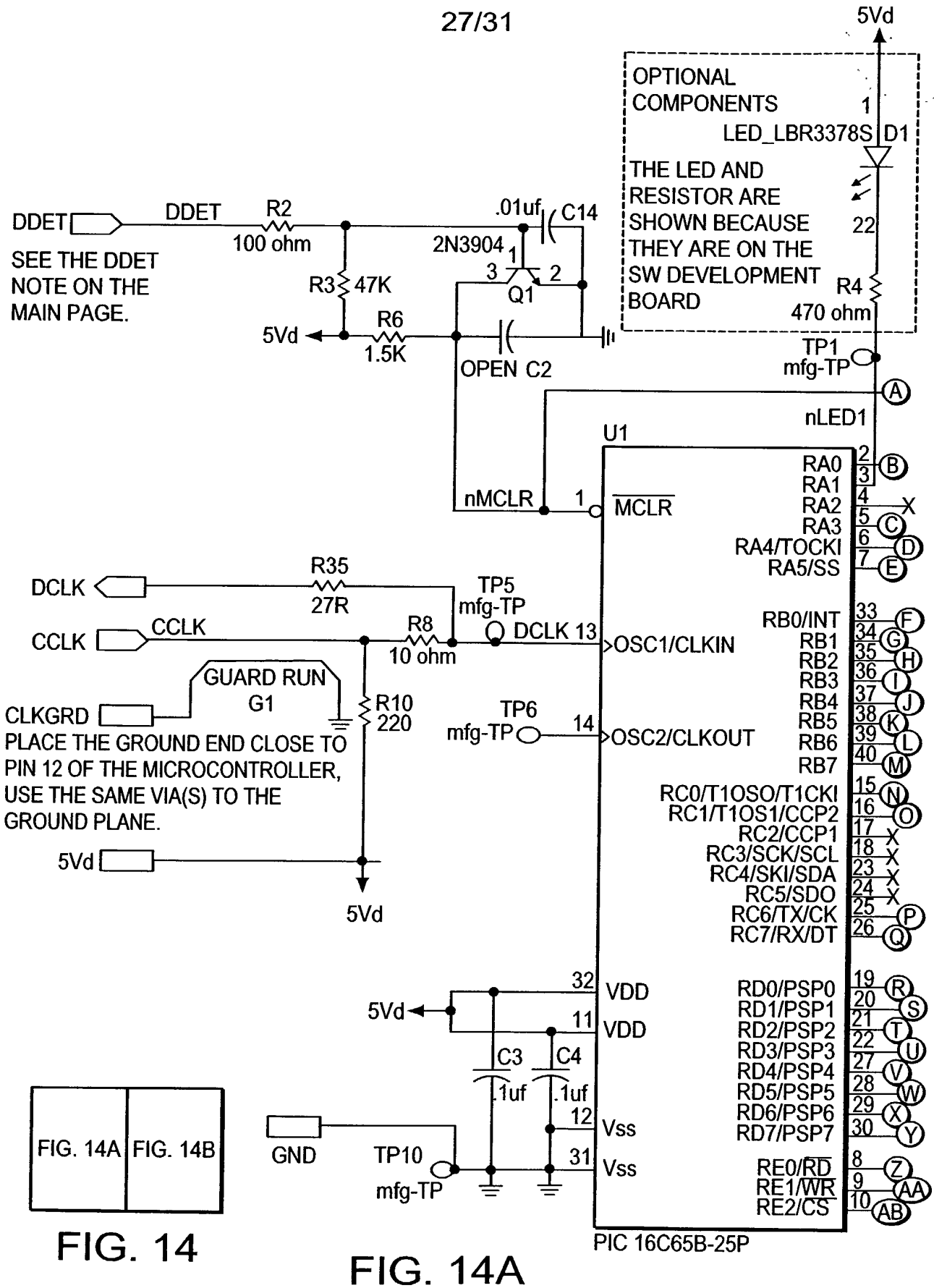


FIG. 14A

FIG. 14A | FIG. 14B

FIG. 14

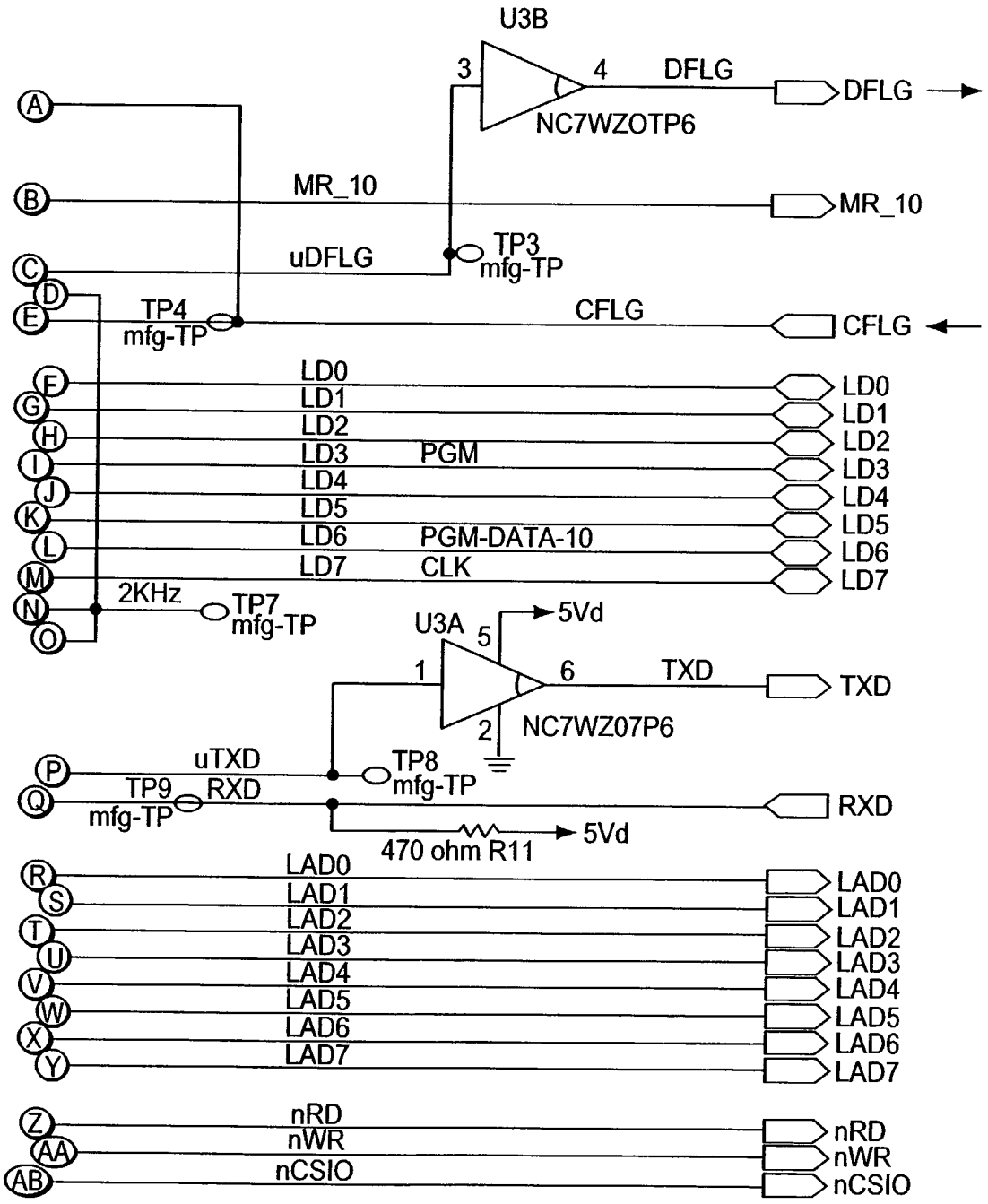
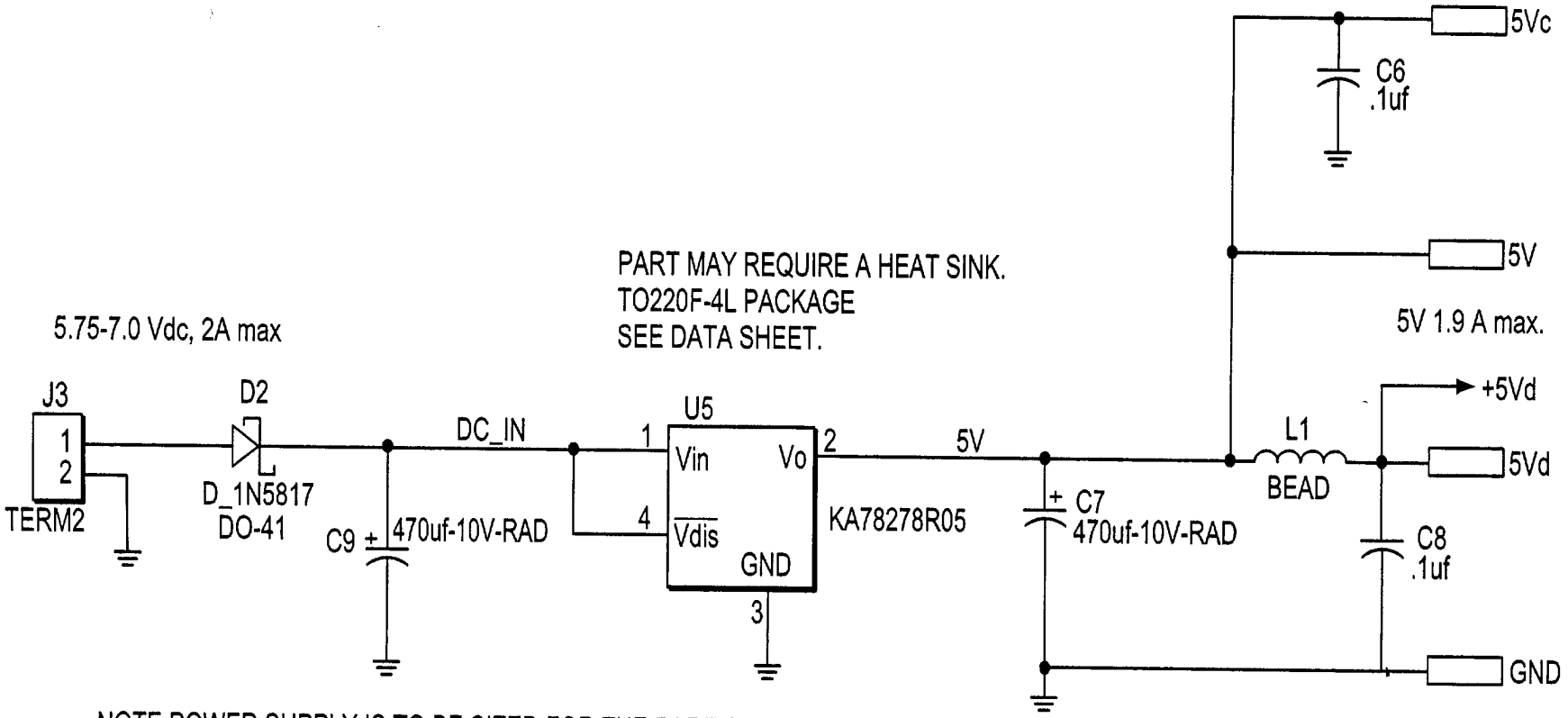

U3B
3
4
DFLG
DFLG
NC7WZOTP6
A
B
MR_10
MR_10
C
uDFLG
TP3
mfg-TP
D
E
TP4
mfg-TP
CFLG
CFLG
F
G
H
I
J
K
L
M
LD0
LD1
LD2
LD3
PGM
LD4
LD5
LD6
PGM-DATA-10
LD7
CLK
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
N
O
2KHz
TP7
mfg-TP
U3A
5
5Vd
1
6
TXD
TXD
2
NC7WZ07P6
P
Q
uTXD
TP8
mfg-TP
TP9
RXD
mfg-TP
RXD
470 ohm R11
5Vd
R
S
T
U
V
W
X
Y
LAD0
LAD1
LAD2
LAD3
LAD4
LAD5
LAD6
LAD7
LAD0
LAD1
LAD2
LAD3
LAD4
LAD5
LAD6
LAD7
Z
AA
AB
nRD
nWR
nCSIO
nRD
nWR
nCSIO

FIG. 14B



NOTE POWER SUPPLY IS TO BE SIZED FOR THE PARTICULAR FLOPPY DISK DRIVE'S MAXIMUM LOAD, ALLOW ~300 mA FOR OTHER LOADS.

SIZING AFFECTS CHOICE OF U5 AND ITS HEATSINK, THE FILTER CAPACITORS, C7, C9 AND THE AC ADAPTER RATING.

FIG. 15

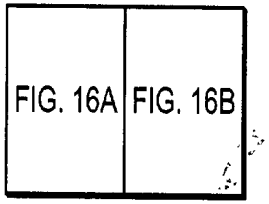


FIG. 16

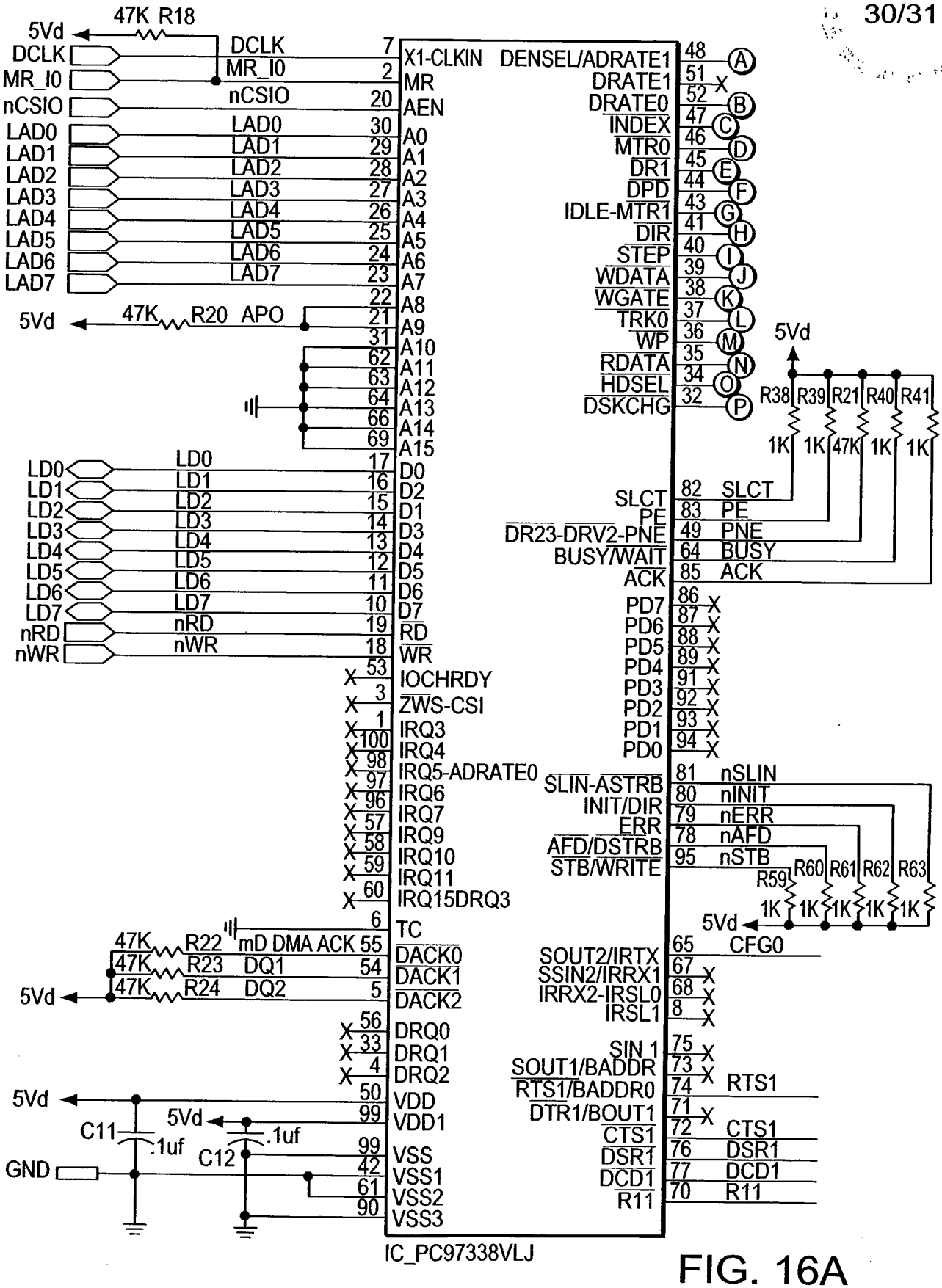

47K R18
5Vd
DCLK
MR_I0
nCSIO
LAD0
LAD1
LAD2
LAD3
LAD4
LAD5
LAD6
LAD7
47K R20 APO
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
nRD
nWR
47K R22 mD DMA ACK
47K R23 DQ1
47K R24 DQ2
C11 .1uf
C12 .1uf
GND
X1-CLKIN
MR
AEN
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
D0
D2
D1
D3
D4
D5
D6
D7
RD
WR
IOCHRDY
ZWS-CSI
IRQ3
IRQ4
IRQ5-ADRATE0
IRQ6
IRQ7
IRQ9
IRQ10
IRQ11
IRQ15DRQ3
TC
DACK0
DACK1
DACK2
DRQ0
DRQ1
DRQ2
VDD
VDD1
VSS
VSS1
VSS2
VSS3
IC_PC97338VLJ
DENSEL/ADRATE1
DRATE1
DRATE0
INDEX
MTR0
DR1
DPD
IDLE-MTR1
DIR
STEP
WDATA
WGATE
TRK0
WP
RDATA
HDSEL
DSKCHG
5Vd
R38 R39 R21 R40 R41
1K 1K 47K 1K 1K
SLCT
PE
DR23-DRV2-PNE
BUSY/WAIT
ACK
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
SLIN-ASTRB
INIT/DIR
ERR
AFD/DSTRB
STB/WRITE
R59 R60 R61 R62 R63
1K 1K 1K 1K 1K
CFG0
SOUT2/IRTX
SSIN2/IRRX1
IRRX2-IRSL0
IRSL1
SIN 1
SOUT1/BADDR
RTS1/BADDR0
DTR1/BOUT1
CTS1
DSR1
DCD1
R11
RTS1
CTS1
DSR1
DCD1
R11

FIG. 16A

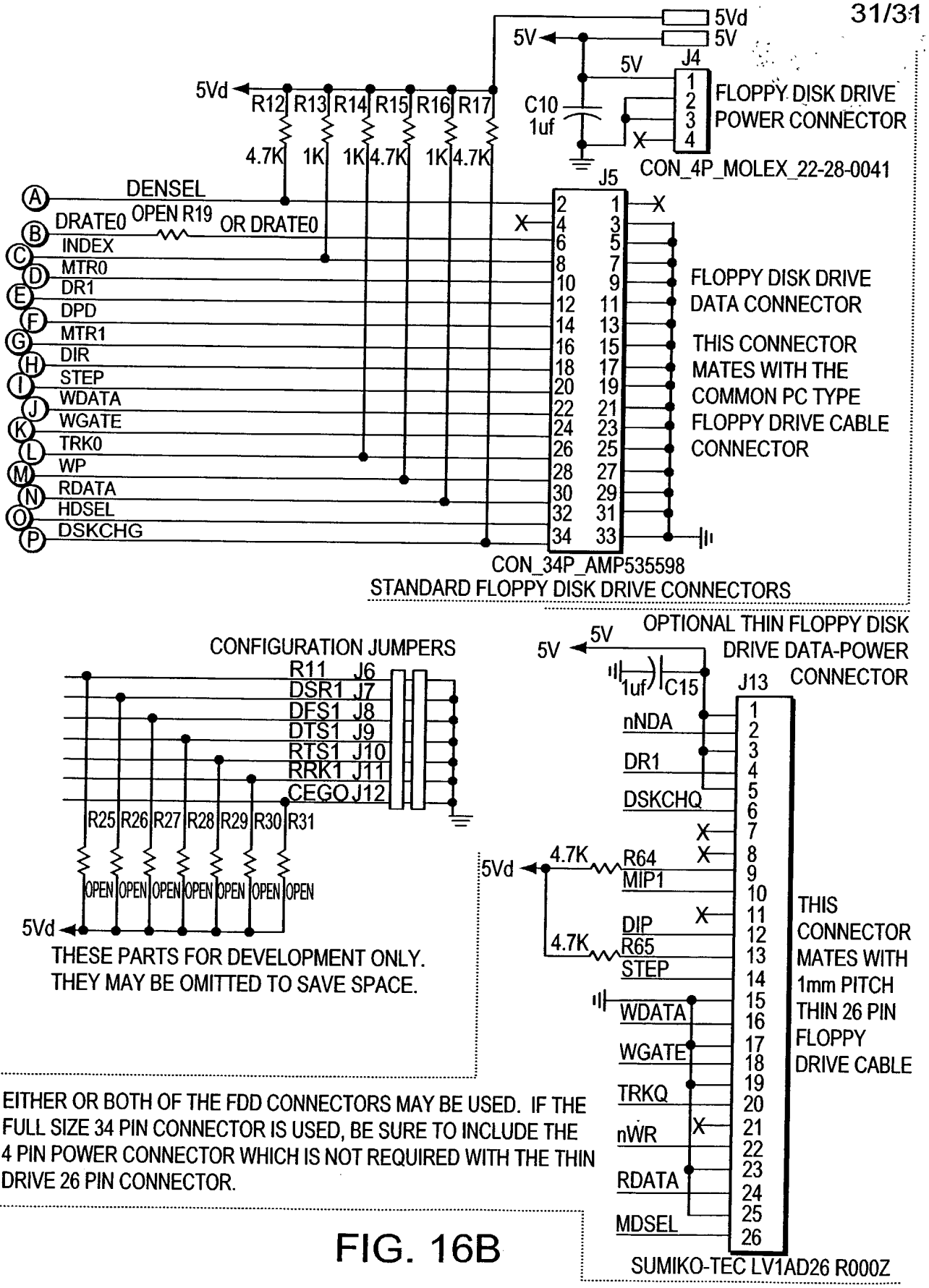

5Vd
5V
J4
FLOPPY DISK DRIVE POWER CONNECTOR
CON_4P_MOLEX_22-28-0041
C10 1uf
R12 R13 R14 R15 R16 R17
4.7K 1K 1K 4.7K 1K 4.7K
DENSEL
DRATE0 OPEN R19 OR DRATE0
INDEX
MTR0
DR1
DPD
MTR1
DIR
STEP
WDATA
WGATE
TRK0
WP
RDATA
HDSEL
DSKCHG
J5
FLOPPY DISK DRIVE DATA CONNECTOR
THIS CONNECTOR MATES WITH THE COMMON PC TYPE FLOPPY DRIVE CABLE CONNECTOR
CON_34P_AMP535598
STANDARD FLOPPY DISK DRIVE CONNECTORS
CONFIGURATION JUMPERS
R11 J6
DSR1 J7
DFS1 J8
DTS1 J9
RTS1 J10
RRK1 J11
CEGO J12
R25 R26 R27 R28 R29 R30 R31
OPEN OPEN OPEN OPEN OPEN OPEN OPEN
THESE PARTS FOR DEVELOPMENT ONLY.
THEY MAY BE OMITTED TO SAVE SPACE.
OPTIONAL THIN FLOPPY DISK DRIVE DATA-POWER CONNECTOR
1uf C15
J13
nNDA
DR1
DSKCHQ
4.7K R64
MIP1
DIP
4.7K R65
STEP
WDATA
WGATE
TRKQ
nWR
RDATA
MDSEL
THIS CONNECTOR MATES WITH 1mm PITCH THIN 26 PIN FLOPPY DRIVE CABLE
SUMIKO-TEC LV1AD26 R000Z
EITHER OR BOTH OF THE FDD CONNECTORS MAY BE USED. IF THE FULL SIZE 34 PIN CONNECTOR IS USED, BE SURE TO INCLUDE THE 4 PIN POWER CONNECTOR WHICH IS NOT REQUIRED WITH THE THIN DRIVE 26 PIN CONNECTOR.

FIG. 16B